I²C Quad Synchronous Step-Down DC/DC Regulator 2 × 600mA, 2 × 400mA

FEATURES

- **Four Independent I²C Controllable Step-Down Regulators (2 × 600mA, 2 × 400mA)**
- **Two I²C Programmable Feedback Voltage Regulators (R600A, R400A): V_{FB} 425mV to 800mV**
- **Two I²C Programmable Output Voltage Regulators (R600B, R400B): V_{OUT} 600mV to 3.775V**
- **Programmable Modes: Pulse Skip, LDO, Burst Mode®, Forced Burst Mode Operation**
- Quiescent Current < 100µA (All Regulators Enabled in LDO Mode)
- Fixed 2.25MHz Switching Frequency (Pulse Skip Mode)
- Slew Limiting Reduces Switching Noise
- Power-On Reset Output for Regulator R600A
- Small, Thermally Enhanced, 20-Lead 3mm × 3mm QFN Package

APPLICATIONS

- Miscellaneous Handheld Applications with Multiple Supply Rails
- Personal Information Appliances
- Wireless and DSL Modems
- Digital Still Cameras
- MP3 Players
- Portable Instruments

DESCRIPTION

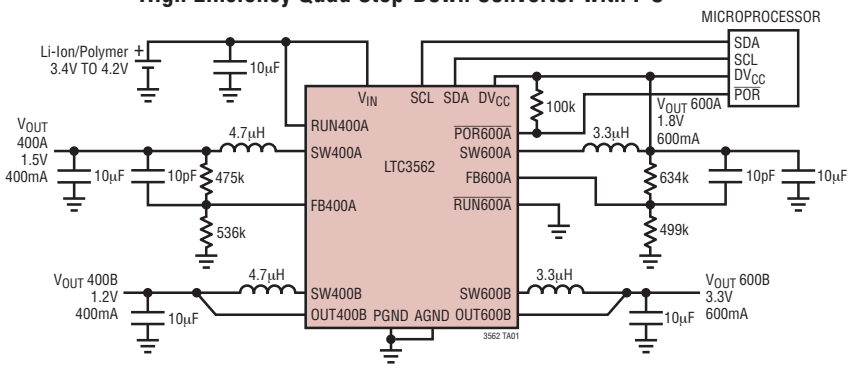
The LTC®3562 is a quad high efficiency monolithic synchronous step-down regulator with an I²C interface. Two regulators are externally adjustable and can have their feedback voltages programmed between 425mV and 800mV in 25mV steps (Type A). The other two regulators are fixed output regulators whose output voltages can be programmed between 600mV and 3.775V in 25mV steps (Type B). All four regulators operate independently and can be put into pulse skip, LDO, Burst Mode operation, or forced Burst Mode operation through I²C control. The Type-A regulators have separate RUN pins that can be enabled if I²C control is unavailable.

The 2.85V to 5.5V input voltage range makes the LTC3562 ideally suited for single Li-Ion battery-powered applications. At low output load conditions, the regulators can be switched into LDO, Burst Mode operation, or forced Burst Mode operation, extending battery life in portable systems. The quiescent current drops to under 100µA with all regulators in LDO mode, and under 0.1µA when all regulators are shut down.

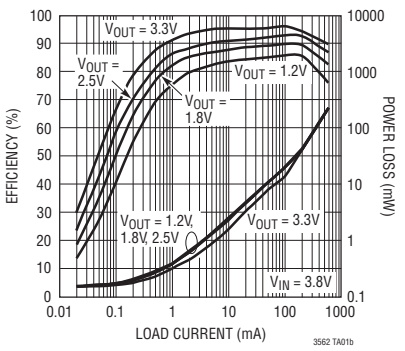
Switching frequency is internally set to 2.25MHz, allowing the use of small surface mount inductors and capacitors. All regulators are internally compensated. The LTC3562 is available in a low profile 3mm × 3mm QFN package.

TYPICAL APPLICATION

High Efficiency Quad Step-Down Converter with I²C



R600x Burst Mode Efficiency and Power Loss vs Load Current

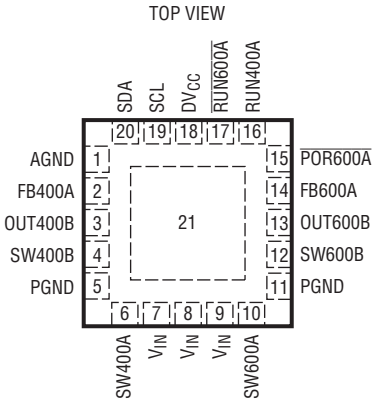


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN} .....–0.3V to 6V
$\overline{RUN600A}$ ..... –0.3V to (V_{IN} + 0.3V)
RUN400A ..... –0.3V to (V_{IN} + 0.3V)
FBx.....–0.3V to 6V
SWx .....–0.3V to 6V
OUTx.....–0.3V to 6V
DV_{CC}, $\overline{POR600A}$, SDA, SCL .....–0.3V to 6V
I_{SW400x} (DC) 600mA
I_{SW600x} (DC) 850mA
Operating Temperature (Note 2).....–40°C to 85°C
Storage Temperature Range.....–65°C to 125°C
Junction Temperature (Note 3) ..... 125°C

PIN CONFIGURATION



UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3562EUD#PBF	LTC3562EUD#TRPBF	LCPV	20-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Input Voltage Range		●	2.7		5.5	V
V_{IN} Input Current (Per Regulator Enabled)	Pulse Skip Mode, I_{OUT} = 0			220		µA
	Burst Mode Operation, I_{OUT} = 0			35	60	µA
	Forced Burst Mode Operation, I_{OUT} = 0			25	40	µA
	LDO Mode, I_{OUT} = 0			24	40	µA
	Shutdown Mode, I_{OUT} = 0, DV_{CC} = 1.8V			0.7	3	µA
V_{IN} Shutdown Current	All Regulators in Shutdown, DV_{CC} = 0V			0.1	1	µA
$\overline{RUN600A}$, RUN400A Input High Threshold		●	1.0			V
$\overline{RUN600A}$, RUN400A Input Low Threshold		●			0.3	V
$\overline{RUN600A}$, RUN400A Input High Current	RUNx = V_{IN}		–1		1	µA
$\overline{RUN600A}$, RUN400A Input Low Current	RUNx = 0V		–1		1	µA
$\overline{POR600A}$ Threshold	Percentage of R600A's Final Output Voltage			–8		%
$\overline{POR600A}$ On-Resistance				16	40	Ω
$\overline{POR600A}$ Delay				231		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Port						
DV_{CC} Operating Voltage		●	1.5		5.5	V
DV_{CC} Operating Current	DV_{CC} = 1.8V, Serial Port Idle				1	µA
DV_{CC} UVLO Threshold Voltage				1		V
V_{IL} SDA, SCL (Low Level Input Voltage)					0.3 • DV_{CC}	V
V_{IH} SDA, SCL (High Level Input Voltage)			0.7 • DV_{CC}			V
V_{OL} SDA (Digital Output Low)	I_{PULLUP} = 3mA			0.08		V
Serial Port Timing (Note 4)						
t_{SCL}	Clock Operating Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Conditions		1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD,DAT(OUT)}$	Data Hold Time		225			ns
$t_{HD,DAT(IN)}$	Input Data Hold Time		0		900	ns
$t_{SU,DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
t_f	Clock Data Fall Time		20		300	ns
t_r	Clock Data Rise Time		20		300	ns
t_{SP}	Spike Suppression Time		50			ns

BUCK DC/DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V, V_{OUTx} = 1.5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulators R600A, R400A, R600B, R400B						
f_{OSC}			1.91	2.25	2.59	MHz
Maximum Duty Cycle	Pulse Skip Mode		100			%
LDO Mode Closed Loop R_{OUT}	LDO Mode			0.25		Ω
Regulators R600A, R600B						
PMOS Switch Current Limit	Pulse Skip Mode		850	1200	1500	mA
PMOS $R_{DS(ON)}$				0.38		Ω
NMOS $R_{DS(ON)}$				0.38		Ω
LDO Mode Open Loop R_{OUT}	LDO Mode			2.2		Ω
Available Output Current	Forced Burst Mode LDO, V_{OUT} = 1.2V		75 50	140		mA mA
SW Pull-Down in Shutdown	Shutdown			2.5		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.8V, V_{OUTx} = 1.5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulators R400A, R400B						
PMOS Switch Current Limit	Pulse Skip Mode		600	800	1000	mA
PMOS $R_{DS(ON)}$				0.5		Ω
NMOS $R_{DS(ON)}$				0.5		Ω
LDO Mode Open Loop R_{OUT}	LDO Mode			3		Ω
SW Pull-Down in Shutdown	Shutdown			2.5		kΩ
Available Output Current	Forced Burst Mode LDO Mode, V_{OUT} = 1.2V		50 50	100		mA mA
Regulators R600A, R400A						
$V_{FB(MAX)}$	DAC = XXX1111, Pulse Skip Mode	●	0.776	0.800	0.824	V
$V_{FB(MIN)}$	DAC = XXX0000, Pulse Skip Mode	●	0.412	0.425	0.438	V
$V_{FB(STEP)}$ (0 to 15)				25		mV
I_{FB}	FB Input Current DAC = XXX1111		 –50	 0	 50	 nA
Regulators R600B, R400B						
$V_{OUT(MIN)}$	V_{IN} = 4V, DAC = 0000000, Pulse Skip Mode	●	0.582	0.600	0.618	V
$V_{OUT(MAX)}$	V_{IN} = 4V, DAC = 1111111, Pulse Skip Mode	●	3.661	3.775	3.889	V
$V_{OUT(STEP)}$ (0 to 127)	V_{IN} = 4V			25		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

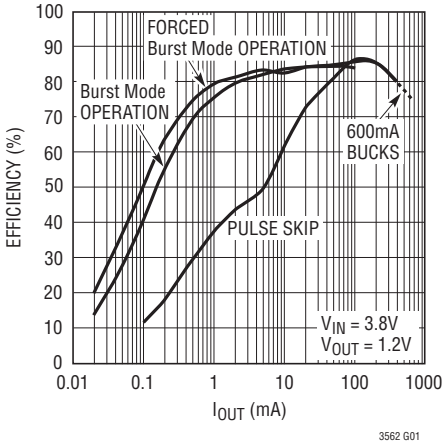
Note 2: The LTC3562E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process control.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

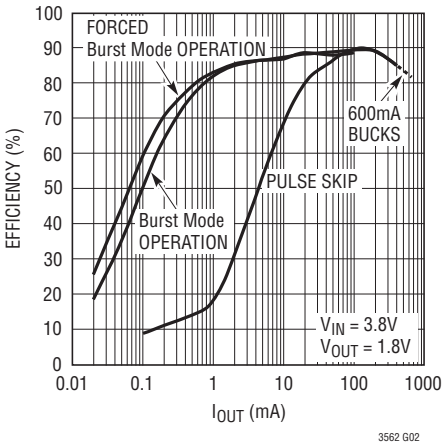
Note 4: The serial port is tested at rated operating frequency. Timing parameters are tested and/or guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

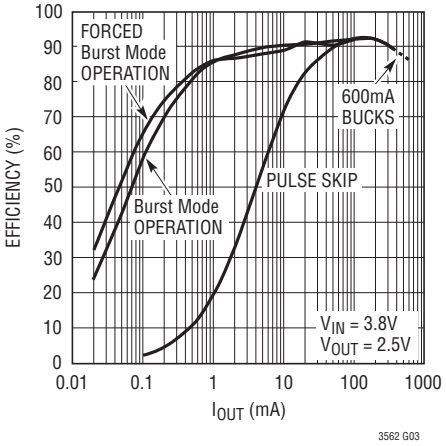
Efficiency vs Load Current



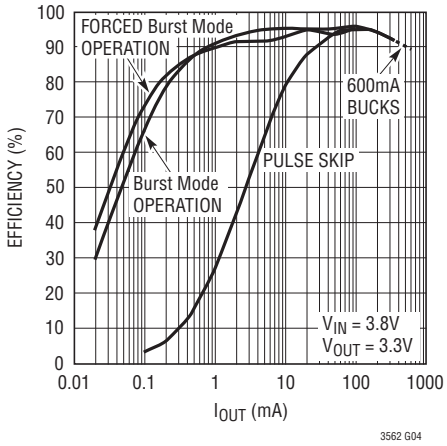
Efficiency vs Load Current



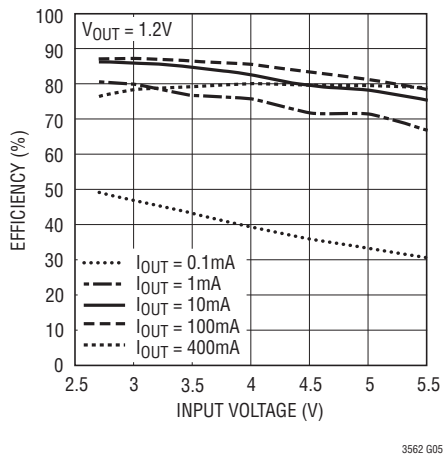
Efficiency vs Load Current



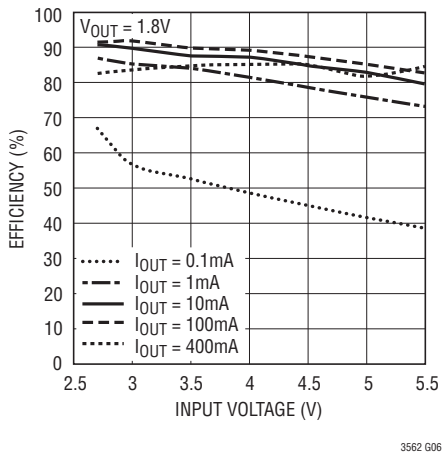
Efficiency vs Load Current



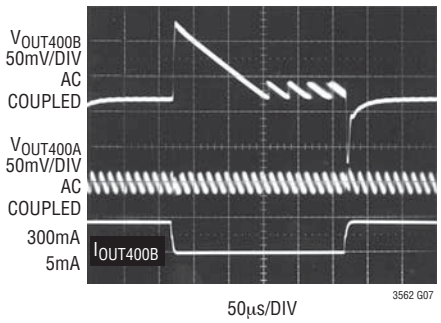
Efficiency vs Input Voltage
Burst Mode Operation



Efficiency vs Input Voltage
Burst Mode Operation



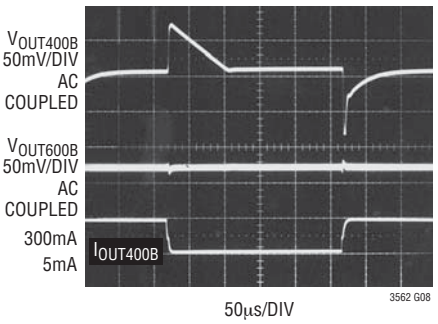
Output Transient
Burst Mode Operation



50µs/DIV

$V_{OUT400B}$ = 1.2V
$V_{OUT400A}$ = 1.2V
$I_{OUT400A}$ = 20mA

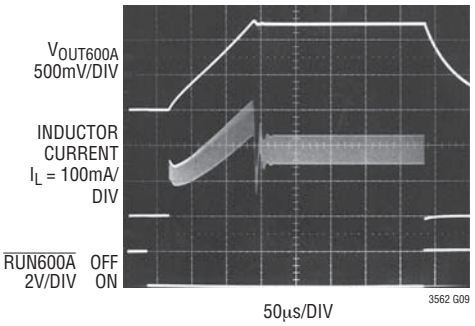
Output Transient
Pulse Skip Mode



50µs/DIV

$V_{OUT400B}$ = 1.8V
$V_{OUT600B}$ = 1.2V
$I_{OUT600B}$ = 15mA

Start-Up Transient
Pulse Skip Mode

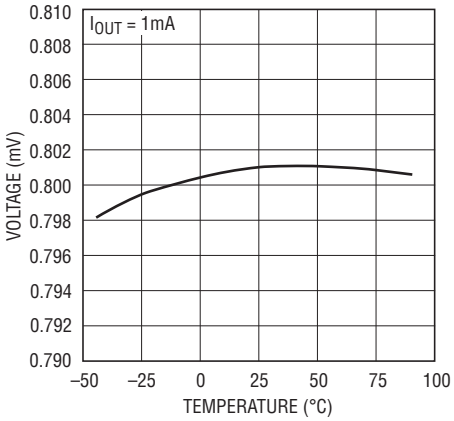


50µs/DIV

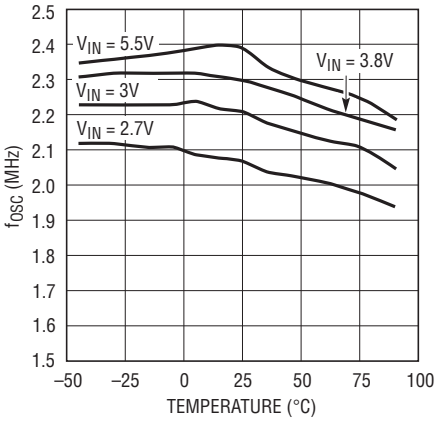
$V_{OUT600A}$ = 1.2V
R_{LOAD} = 6Ω

TYPICAL PERFORMANCE CHARACTERISTICS

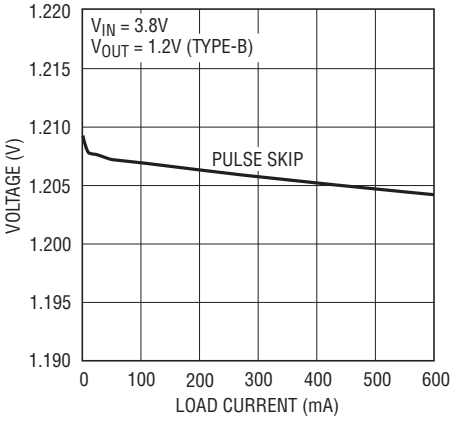
R600A Feedback Voltage vs Temperature



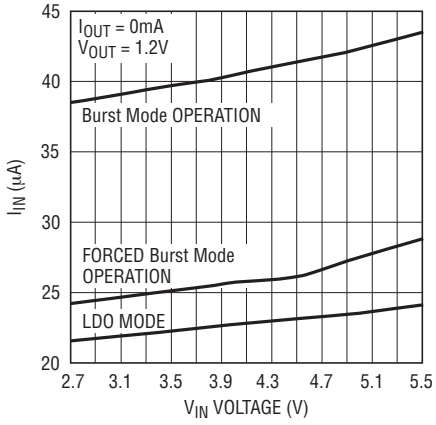
Oscillator Frequency vs Temperature



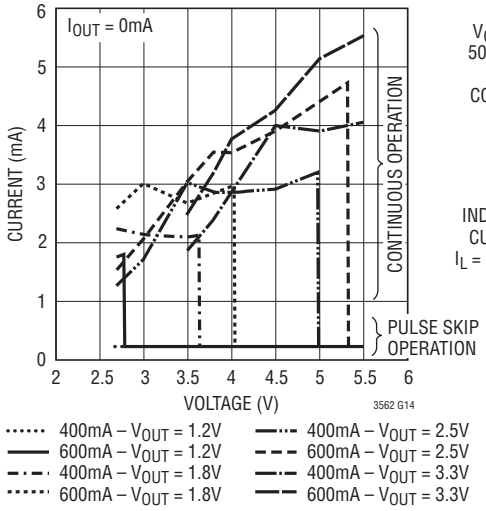
Output Voltage vs Load Current (B Version)



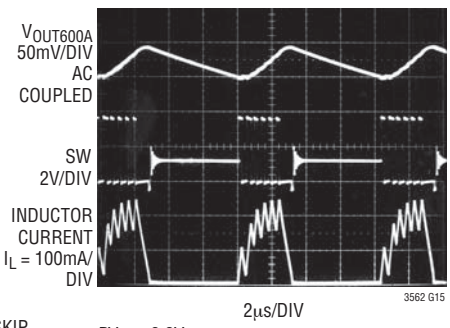
Dynamic Supply Current vs Input Voltage



Dynamic Supply Current vs Input Voltage



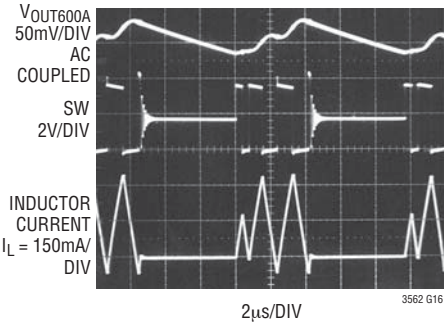
Burst Mode Operation



2µs/DIV

PV_{IN} = 3.8V
LOAD = 50mA

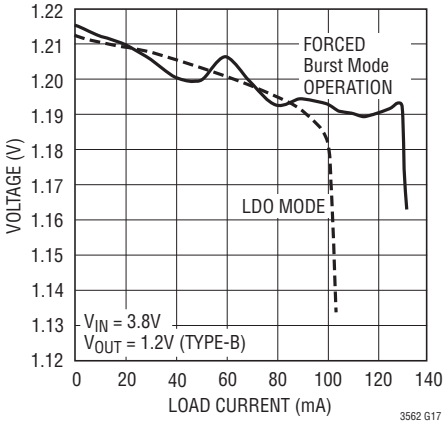
Forced Burst Mode Operation



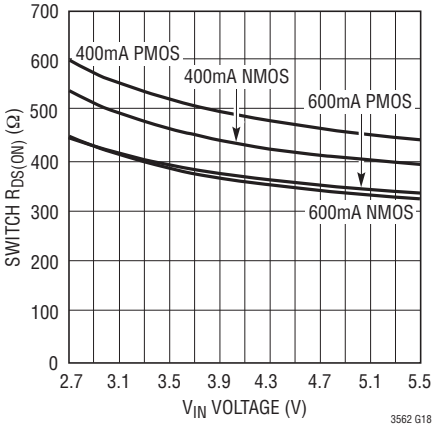
2µs/DIV

PV_{IN} = 3.8V
LOAD = 50mA

Output Voltage vs Load Current



Switch $R_{DS(ON)}$ vs Input Voltage



PIN FUNCTIONS

AGND (Pin 1): Analog Ground Pin. All small-signal components should connect to this ground, which in turn connects to PGND at one point.

FB400A (Pin 2): Feedback Pin for R400A. When the control loop is complete, this pin servos to 1 of 16 possible set-points based on the programmed value from the I^2C serial port (see Table 4).

OUT400B (Pin 3): Output Voltage Feedback Pin for R400B. An I^2C programmable internal resistor divider divides the output voltage down for comparison to the internal reference voltage. This pin converges to 1 of 128 possible set-points based on the programmed value from the I^2C serial port (see Tables 5 and 6). This node must be bypassed to GND with a 10µF or greater ceramic capacitor.

SW400B (Pin 4): Switch Node Connection to the Inductor for R400B. This pin connects to the drains of the internal power MOSFET switches of R400B.

PGND (Pins 5, 11): Power Ground Pin. Connect this pin closely to the (–) terminal of C_{IN}.

SW400A (Pin 6): Switch Node Connection to the Inductor for R400A. This pin connects to the drains of the internal power MOSFET switches of R400A.

V_{IN} (Pins 7, 8, 9): Input Supply Pin. This pin must be closely decoupled to GND with a 10µF or greater ceramic capacitor.

SW600A (Pin 10): Switch Node Connection to the Inductor for R600A. This pin connects to the drains of the internal power MOSFET switches of R600A.

SW600B (Pin 12): Switch Node Connection to the Inductor for R600B. This pin connects to the drains of the internal power MOSFET switches of R600B.

OUT600B (Pin 13): Output Voltage Feedback Pin for R600B. An I^2C programmable internal resistor divider divides the output voltage down for comparison to the internal reference voltage. This pin converges to 1 of 128 possible set-points based on the programmed value from the I^2C serial port (see Tables 5 and 6). This node must be bypassed to GND with a 10µF or greater ceramic capacitor.

FB600A (Pin 14): Feedback Pin for R600A. When the control loop is complete, this pin servos to 1 of 16 possible set-points based on the programmed value from the I^2C serial port (see Table 4).

$\overline{\text{POR600A}}$ (Pin 15): Power-On Reset for R600A. This open-drain output goes high impedance after a 230ms delay after the output of R600A reaches 92% of its regulation voltage. This output gets pulled to GND whenever R600A falls below 92% of its regulation voltage.

RUN400A (Pin 16): Enable Pin for R400A, Active High. Apply a voltage greater than 1V to enable this regulator.

$\overline{\text{RUN600A}}$ (Pin 17): Enable Pin for R600A, Active Low. Apply a voltage less than 0.3V to enable this regulator.

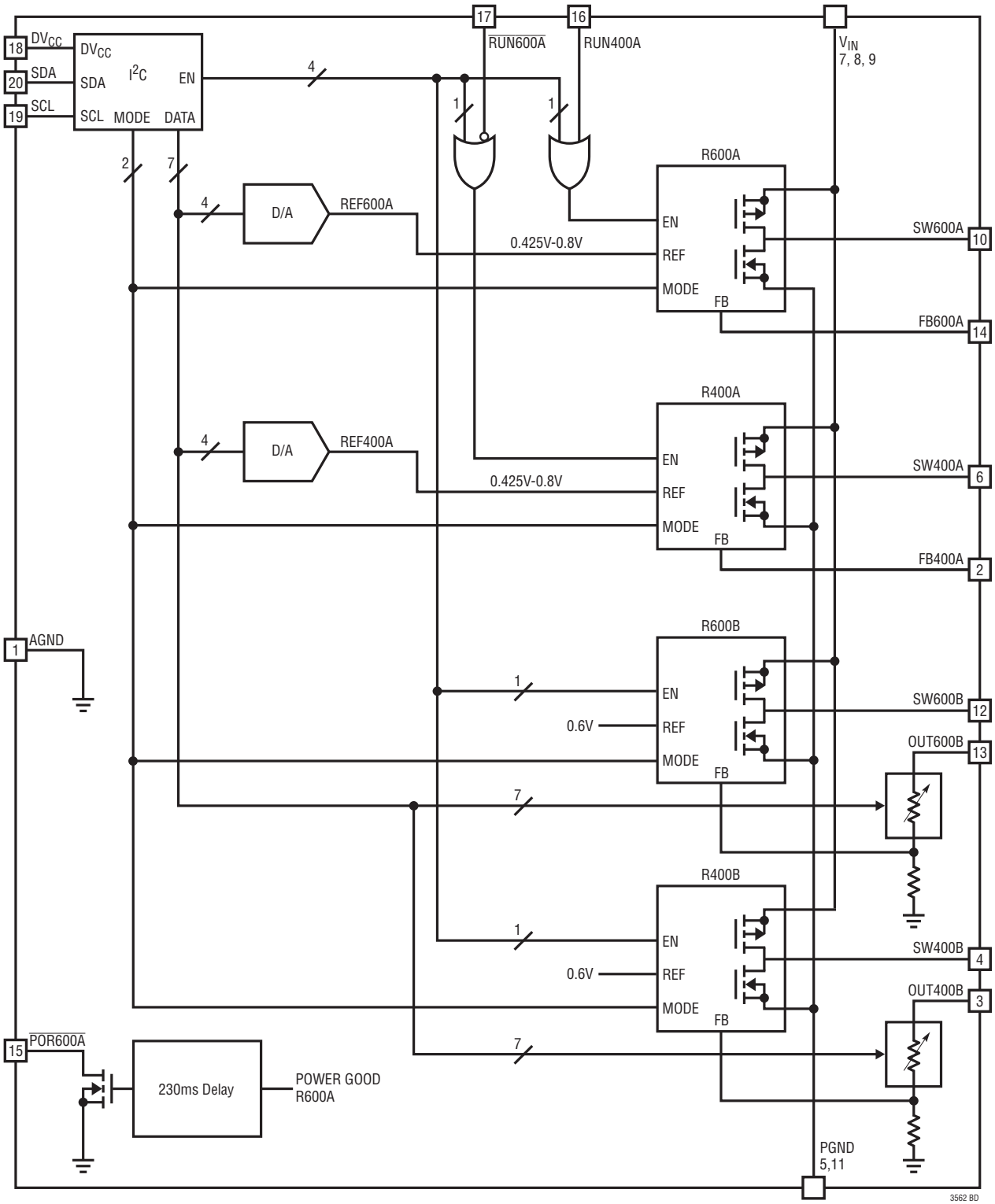
DV_{CC} (Pin 18): Supply Voltage for I^2C Lines. This pin sets the logic reference level of the LTC3562. A UVLO circuit on the DV_{CC} pin forces all registers to a default setting whenever DV_{CC} is < 1V. Bypass to GND with a 0.1µF capacitor.

SCL (Pin 19): I^2C Clock Input. Serial data is shifted one bit per clock to control the LTC3562. The logic level for SCL is referenced to DV_{CC}.

SDA (Pin 20): I^2C Data Input. The logic level for SDA is referenced to DV_{CC}.

Exposed Pad (Pin 21): Ground. Must be soldered to PCB ground for electrical contact and optimum thermal performance.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC3562 is a highly integrated power management IC that contains four I²C controllable, monolithic, high efficiency step-down regulators. Two regulators provide up to 600mA of output current and the other two regulators produce up to 400mA. All four regulators are 2.25MHz, constant-frequency, current mode switching regulators that can be independently controlled through I²C. All regulators are internally compensated eliminating the need for external compensation components.

The LTC3562 offers two different types of adjustable step-down regulators. The two Type-A regulators (R600A, R400A) can have the feedback voltages adjusted through I²C from 425mV to 800mV in 25mV increments. The two Type-B regulators (R600B, R400B) can have the output voltages adjusted through I²C control from 600mV to 3.775V in 25mV increments.

All four converters support 100% duty cycle operation (low dropout mode) when their input voltage drops very close to their output voltage. To suit a variety of applications, four selectable mode functions are available on the LTC3562's step-down regulators to trade-off noise for efficiency.

At moderate to heavy loads, the constant-frequency pulse skip mode provides the lowest output switching noise solution. At lighter loads, either Burst Mode operation, forced Burst Mode operation or LDO mode may be selected to optimize efficiency. The switching regulators also include soft-start to limit inrush current when powering on, short-circuit current protection, and switch node slew limiting circuitry to reduce radiated EMI. No external compensation components are required.

V_{FB} Adjustable (Type-A) Regulators

The two Type-A step-down regulators (R600A and R400A) have individual programmable feedback servo voltages via I²C control. Given a particular feedback servo voltage, the output voltage is programmed using a resistor divider from the switching regulator output connected to the feedback pins (Figure 1). The output voltage is related to the feedback servo voltage by the following equation:

$$V_{OUTxA} = V_{FBxA}\left(\frac{R1}{R2}+1\right)$$

Through I²C control, V_{FBxA} can be programmed from 800mV (full scale) down to 425mV in 25mV increments. When the RUN pins ($\overline{RUN600A}$ and RUN400A) are used to activate these regulators, the default feedback servo voltage is set to 800mV.

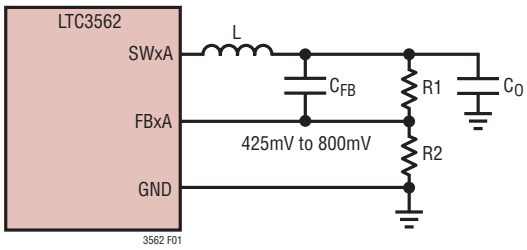


Figure 1. Type-A Regulator Application Circuit

Typical values for R2 are in the range of 40k to 1MΩ. The capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

Regulators R600A and R400A have individual RUN pins that can enable the regulators without accessing the I²C port. The $\overline{RUN600A}$ and RUN400A pins are OR'ed with the enable signals coming from the I²C port (refer to the Block Diagram) such that regulators R600A and R400A can be enabled if the I²C port is unavailable. The $\overline{RUN600A}$ pin is active low and the RUN400A pin is active high.

When the RUN pins are activated, the Type-A regulators are enabled in a default setting. The default mode for the regulators is pulse skip mode and the default feedback servo voltage setting is 800mV. Once enabled with these default settings, the settings can always be changed on the fly through I²C once the I²C terminal is available.

The maximum operating output current of regulators R600A and R400A are 600mA and 400mA, respectively.

OPERATION

V_{OUT} Adjustable (Type-B) Regulators

Unlike the Type-A regulators, the two Type-B regulators do not require an external resistor divider network to program its output voltage. Regulators R600B and R400B have feedback resistor networks internal to the chip whose values can be adjusted through I^2C control. These internal feedback resistors can be configured such that the output voltages can be programmed directly. The output voltages can be programmed from 600mV to 3.775V in 25mV increments.

Pins OUT600B and OUT400B are feedback sense pins that connect to the top of the internal resistor divider networks. These output pins should sense the output voltages of the regulators right at the output capacitor C_O (after the inductor), as illustrated in Figure 2.

The maximum operating current for regulators R600B and R400B are 600mA and 400mA, respectively. The Type-B regulators do not have individual run pins as do the Type-A regulators. Thus regulators R600B and R400B can only be enabled through control of the I^2C port. When the part initially powers up, the Type-B regulators default to shutdown mode and remain disabled until programmed through I^2C.

Regulator Operating Modes

All of the LTC3562's switching regulators include four possible operating modes to meet the noise/power needs of a variety of applications.

In pulse skip mode, an internal latch is set at the start of every cycle which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse skip mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW) goes high impedance and the switch node voltage will "ring." This is discontinuous mode operation, and is normal behavior for a switching regulator. At very light loads in pulse skip mode, the switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle ($V_{OUT} > V_{IN}/2$) it is possible for the inductor current to reverse at light loads, causing the step-down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a couple mA.

In forced Burst Mode operation, the switching regulators use a constant-current algorithm to control the inductor current. By controlling the inductor current directly and using a hysteretic control loop, both noise and switching losses are minimized. In this mode output power is limited. While operating in forced Burst Mode operation,

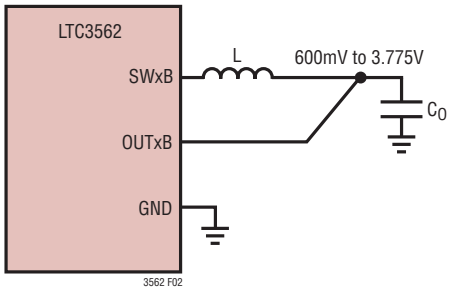


Figure 2. Type-B Regular Application Circuit

OPERATION

the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down converter then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the regulator's circuitry is powered down, helping conserve battery power and increase efficiency. When the output voltage drops below a predetermined value, the switching regulator circuitry is powered on and another burst cycle begins. The duration for which the regulator operates in sleep mode depends on the load current. The sleep time decreases as the load current increases. Forced Burst Mode operation has a maximum deliverable output current of about 140mA for the 600mA regulators and 100mA for the 400mA regulators. Beyond the maximum deliverable output current, the step-down switching regulator will not enter sleep mode and the output will drop out of regulation. Forced Burst Mode operation provides a significant improvement in efficiency at light loads at the expense of higher output ripple when compared to pulse skip mode. For many noise-sensitive systems, forced Burst Mode operation might be undesirable at certain times (i.e., during a transmit or receive cycle of a wireless device), but highly desirable at others (i.e., when the device is in low power standby mode). The I^2C port can be used to enable or disable forced Burst Mode operation at any time, offering both low noise and low power operation when they are needed.

In Burst Mode operation, the switching regulator automatically switches between fixed frequency pulse skip operation and hysteretic control as a function of the load current. At light loads the regulators operate in hysteretic mode and at heavy loads they operate in constant-frequency mode. The constant-frequency mode provides the same output ripple and efficiency as pulse skip mode while hysteretic mode provides slightly lower output ripple than forced Burst Mode operation at the expense of slightly lower efficiency.

Finally, the switching regulators have an LDO mode that gives a DC option for regulating their output voltages. In LDO mode, the switching regulators are converted to linear regulators and deliver continuous power from their SWx pins through their respective inductors. This mode gives the lowest possible output noise as well as low quiescent current at light loads.

Dropout Operation

It is possible for V_{IN} to approach a switching regulator's programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize the battery in-rush current. A soft-start cycle occurs whenever a given switching regulator is enabled, or after a fault condition has occurred (thermal shutdown). A soft-start cycle is not triggered by changing operating modes. This allows seamless output operation when transitioning between Burst Mode operation, forced Burst Mode operation, pulse skip mode or LDO mode.

Switching Slew Rate Control

The step-down switching regulators contain new patent pending circuitry to limit the slew rate of the switch node (SWx). This new circuitry is designed to transition the switch node over a period of a couple nanoseconds, significantly reducing radiated EMI and conducted supply noise, while keeping efficiency high.

Step-Down Switching Regulator in Shutdown

The step-down switching regulators are in shutdown when not enabled for operation. In shutdown, all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply, leaving only a few nano-amps of leakage current. The step-down switching regulator outputs are individually pulled to ground through a 2k resistor on the switch pin (SWx) when in shutdown.

OPERATION

I²C Interface

The LTC3562 may communicate with a host (master) using the standard I²C 2-wire interface. The Timing Diagram in Figure 4 shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus Accelerator, are required on these lines. The LTC3562 is a receive-only (slave) device. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the microcontroller generating the I²C signals.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I²C serial port is cleared and the two switching Type-A regulators are set to full scale.

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

START and STOP Conditions

A bus master signals the beginning of a communication to a slave device by transmitting a start condition. A start condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I²C device.

Byte Format

Each byte sent to the LTC3562 must be 8 bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3562. The data should be sent to the LTC3562 most significant bit (MSB) first.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave (LTC3562) lets the master know that the latest byte of information was received. The Acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock cycle. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable low during the high period of this clock pulse.

Slave Address Byte

The LTC3562 responds to only one 7-bit address which has been factory programmed to 11001010. The eighth bit of the address byte (R/W) must be 0 for the LTC3562 to recognize the address since it is a write-only device. This effectively forces the address to be 8 bits long where the least significant bit of the address is 0. If the correct 7-bit address is given but the R/W bit is 1, the LTC3562 will not respond.

Sub-Address Byte

The sub-address byte uses bits A7 through A4 to specify the regulator(s) being programmed by that particular three-byte sequence (refer to Table 2). A specific regulator gets programmed if its corresponding sub-address bit is high, whereas the regulator ignores the 3-byte sequence if its sub-address bit is low. Note that multiple regulators can be programmed by the same 3-byte sequence if more than one of the sub-address bits are high. Bits A1 and A0 of the sub-address byte are used to program the operating mode (Table 3). Bits A3 and A2 of the sub-address byte are not used.

Data Byte

The data byte only affects the regulators that are specified to be programmed by the sub-address byte. The MSB of the data byte (B7) is used to enable or disable the regulator(s) being programmed. A high B7 indicates an enable command, whereas a low B7 indicates a shutdown command.

OPERATION

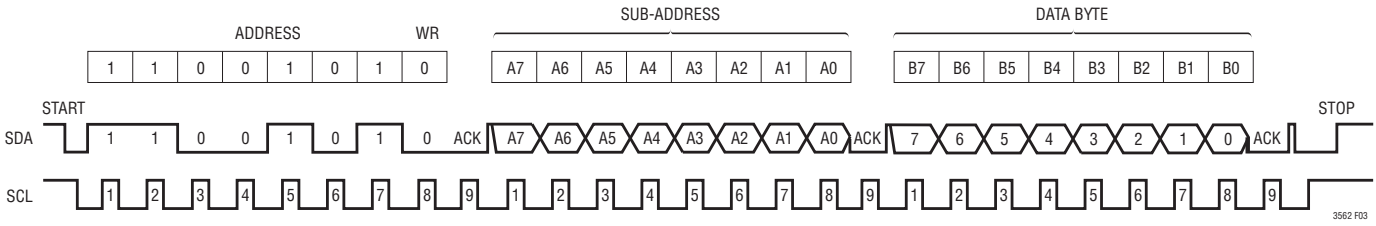


Figure 3. Bit Assignments

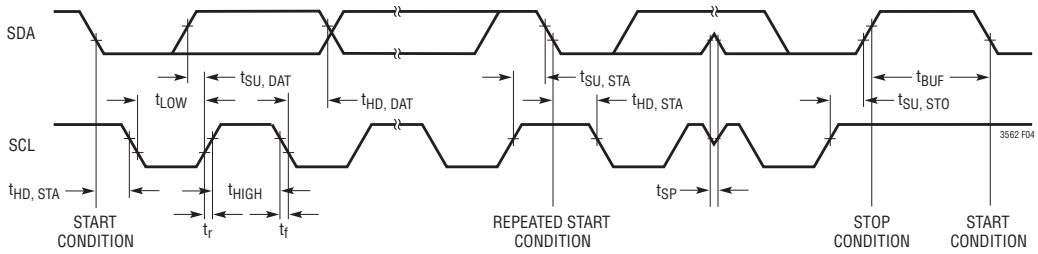


Figure 4. Timing Parameters

Table 1. Write Word Protocol Used by the LTC3562

1	7	1	1	8	1	8	1	1
S	Slave Address	WR	A	*Sub-Address	A	Data Byte	A	P**

S = Start Condition, WR = Write Bit = 0, A = Acknowledge, P = Stop Condition

* The sub-address uses only the first four most significant bits, A7, A6, A5, and A4, for sub-addressing. The two least significant bits, A1 and A0, are used to program the regulator operating mode.

**Stop can be delayed until all of the data registers have been written.

Table 2. Sub-Address and Data Byte Mapping

SUB-ADDRESS BYTE								DATA BYTE							
A7	A6	A5	A4	A3	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
PROGRAM R600A	PROGRAM R400A	PROGRAM R600B	PROGRAM R400B	NOT USED		REGULATOR OPERATING MODE (SEE TABLE 3)		ENABLE REGULATOR	DAC CODE (See Tables 4, 5 and 6)						

OPERATION

If a Type-A regulator is being programmed, then bits B3 through B0 program the DAC that controls the regulator's feedback servo voltage. This 4-bit sequence programs the feedback voltage from 425mV to 800mV in 25mV increments (Table 4). Bits B6 through B4 are not used when programming a Type-A regulator.

If a Type-B regulator is being programmed, then bits B6 through B0 program the DAC that controls the regulator's output voltage. This 7-bit sequence programs the output voltage from 600mV to 3.775V in 25mV increments (Tables 5 and 6).

Bus Write Operation

The master initiates communication with the LTC3562 with a start condition and a 7-bit address followed by the write bit R/W = 0. If the address matches that of the LTC3562, the LTC3562 returns an Acknowledge. The master should then deliver the sub-address byte for the regulator(s) being programmed. Again the LTC3562 acknowledges and then the data byte is delivered starting with the most significant bit. The data byte and the two mode bits in the sub-address byte are transferred to an internal holding latch for each programmed regulator upon the return of an Acknowledge. After the sub-address byte and data byte have been transferred to the LTC3562, the master may terminate the communication with a stop condition. Alternatively, a repeat-start condition can be initiated by the master and the entire sequence can be repeated, this time accessing a different sub-address code to program another regulator. Likewise, the master can also initiate a Repeat-Start so that another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3562's regulators will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global stop condition can be sent and the LTC3562 will update its regulators with the data that it had received.

In certain circumstances the data on the I^2C bus may become corrupted. In these cases the LTC3562 responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3562 has been successfully addressed and is receiving data when a stop condition mistakenly occurs. The LTC3562 will ignore this stop condition and will not respond until a new start condition, correct address, new set of data and stop condition are transmitted.

Likewise, with only one exception, if the LTC3562 was previously addressed and sent valid data but not updated with a Stop, it will respond to any Stop that appears on the bus, independent of the number of Repeat-Starts that have occurred. If a Repeat-Start is given and the LTC3562 successfully acknowledges its address, it will not respond to a Stop until all three bytes of the new data have been received and acknowledged.

I^2C Examples

To program R600A in forced Burst Mode operation with its feedback servo voltage set to 600mV:

Sub-Address Byte – 1000XX10
Data Byte – 1XXX0111

To program R600B and R400B in LDO mode with their output voltages set to 1.250V:

Sub-Address Byte – 0011XX01
Data Byte – 10011010

To put the entire chip in shutdown and disable all regulators:

Sub-Address Byte – 1111XXXX
Data Byte – 0XXXXXXX

Disabling the I^2C Port

The I^2C serial port can be disabled by grounding the DV_{CC} pin. In this mode, regulators R600A and R400A can only be activated through the individual logic input pins $\overline{RUN600A}$ and RUN400A. Disabling the I^2C port also resets the feedback servo voltages to the default setting of 0.8V.

Note that if the I^2C port gets disabled while a Type-A regulator is enabled and its RUN pin is activated, the regulator will remain enabled and its feedback voltage will immediately be reset to the default setting of 0.8V. If the I^2C port gets disabled and the RUN pins are not activated, then the regulators will immediately go into shutdown mode. Since regulators R600B and R400B do not have RUN pins, they immediately go into shutdown once the I^2C port gets disabled.

OPERATION

Table 3. Regulator Operating Modes

A1	A0	REGULATOR MODE
0	0	Pulse Skip Mode
0	1	LDO Mode
1	0	Forced Burst Mode Operation
1	1	Burst Mode Operation

Table 4. Type-A Regulator Servo Voltage Programming

B3	B2	B1	B0	TYPE-A REGULATOR SERVO (FEEDBACK) VOLTAGE
0	0	0	0	0.425
0	0	0	1	0.450
0	0	1	0	0.475
0	0	1	1	0.500
0	1	0	0	0.525
0	1	0	1	0.550
0	1	1	0	0.575
0	1	1	1	0.600
1	0	0	0	0.625
1	0	0	1	0.650
1	0	1	0	0.675
1	0	1	1	0.700
1	1	0	0	0.725
1	1	0	1	0.750
1	1	1	0	0.775
1	1	1	1	0.800

$\overline{\text{POR600A}}$ Pin

The $\overline{\text{POR600A}}$ pin is an open-drain output used to indicate that regulator R600A has been enabled and has reached its final voltage. $\overline{\text{POR600A}}$ remains low impedance until regulator R600A reaches 92% of its regulation value. A 230ms delay is included to allow a system microcontroller ample time to reset itself. $\overline{\text{POR600A}}$ may be used as a power on reset to the microprocessor powered by regulator R600A or may be used to enable regulator R400A for supply sequencing. $\overline{\text{POR600A}}$ is an open drain output and requires a pull-up resistor to the output voltage of regulator R600A or another appropriate power source.

Table 5. Type-B Regulator Base Output Voltage Programming

B6	B5	B4	B3	B2	TYPE-B REGULATOR BASE OUTPUT VOLTAGE
0	0	0	0	0	0.600
0	0	0	0	1	0.700
0	0	0	1	0	0.800
0	0	0	1	1	0.900
0	0	1	0	0	1.000
0	0	1	0	1	1.100
0	0	1	1	0	1.200
0	0	1	1	1	1.300
0	1	0	0	0	1.400
0	1	0	0	1	1.500
0	1	0	1	0	1.600
0	1	0	1	1	1.700
0	1	1	0	0	1.800
0	1	1	0	1	1.900
0	1	1	1	0	2.000
0	1	1	1	1	2.100
1	0	0	0	0	2.200
1	0	0	0	1	2.300
1	0	0	1	0	2.400
1	0	0	1	1	2.500
1	0	1	0	0	2.600
1	0	1	0	1	2.700
1	0	1	1	0	2.800
1	0	1	1	1	2.900
1	1	0	0	0	3.000
1	1	0	0	1	3.100
1	1	0	1	0	3.200
1	1	0	1	1	3.300
1	1	1	0	0	3.400
1	1	1	0	1	3.500
1	1	1	1	0	3.600
1	1	1	1	1	3.700

Table 6. Type-B Regulator Incremental Output Voltage Programming

B1	B0	TYPE-B REGULATOR INCREMENTAL OUTPUT VOLTAGE
0	0	+0.000
0	1	+0.025
1	0	+0.050
1	1	+0.075

APPLICATIONS INFORMATION

Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The step-down converters are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for the lower power switching regulators R400A and R400B and 3.3µH is recommended for the more powerful switching regulators R600A and R600B. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time, but will reduce the available output current. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resist-ance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy™ materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price versus size, performance, and any radiated EMI requirements than on what the LTC3562 requires to operate.

The inductor value also has an effect on Burst Mode and forced Burst Mode operations. Lower inductor values will cause the Burst Mode and forced Burst Mode switching frequencies to increase.

Table 7 shows several inductors that work well with the LTC3562's general purpose regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 7. Recommended Inductors

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE (mm) (L × W × H)	MANUFACTURER
DB318C	4.7	1.07	0.1	3.8 × 3.8 × 1.8	Toko
	3.3	1.20	0.07	3.8 × 3.8 × 1.8	www.toko.com
D312C	4.7	0.79	0.24	3.6 × 3.6 × 1.2	
	3.3	0.90	0.20	3.6 × 3.6 × 1.2	
DE2812C	4.7	1.15	0.13*	3.0 × 2.8 × 1.2	
	3.3	1.37	0.105*	3.0 × 2.8 × 1.2	
DE2818C	4.7	1.25	0.072*	3.0 × 2.8 × 1.8	
	3.3	1.45	0.052*	3.0 × 2.8 × 1.8	
CDRH3D16	4.7	0.9	0.11	4 × 4 × 1.8	Sumida
	3.3	1.1	0.085	4 × 4 × 1.8	www.sumida.com
CDRH2D11	4.7	0.5	0.17	3.2 × 3.2 × 1.2	
	3.3	0.6	0.123	3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1	
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper
	3.3	1.59	0.113	3.1 × 3.1 × 1.8	www.cooperet.com
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
	3.3	0.97	0.165	3.1 × 3.1 × 1.2	
SD12	4.7	1.29	0.117*	5.2 × 5.2 × 1.2	
	3.3	1.42	0.104*	5.2 × 5.2 × 1.2	
SD10	4.7	1.08	0.153*	5.2 × 5.2 × 1.0	
	3.3	1.31	0.108*	5.2 × 5.2 × 1.0	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coil Craft
	3.3	1.3	0.13	3.0 × 3.0 × 1.5	www.coilcraft.com

* Typical DCR

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at the switching regulator outputs as well as the input supply. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for most applications. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. The input supply should be bypassed with a 10µF capacitor, or greater. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer

APPLICATIONS INFORMATION

very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 8 shows a list of several ceramic capacitor manufacturers.

Table 8. Recommended Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Printed Circuit Board Layout Considerations

To deliver maximum current under all conditions, it is critical that the exposed metal pad on the backside of the LTC3562 package be soldered to the PC board ground. Correctly soldered to a 2500mm^2 double-sided 1oz. copper board, the LTC3562 has a thermal resistance of less than 68°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in higher thermal resistances.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitors, inductors, and output capacitors be as close to the LTC3562 as possible and that there be an unbroken ground plane under the LTC3562 and all of its external high frequency components. High frequency currents on the LTC3562 tend to find their way along the ground plane in a myriad of paths ranging from directly back to a mirror path beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur. There should be a group of vias directly under the grounded backside of the package leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be on the second layer of the PC board.

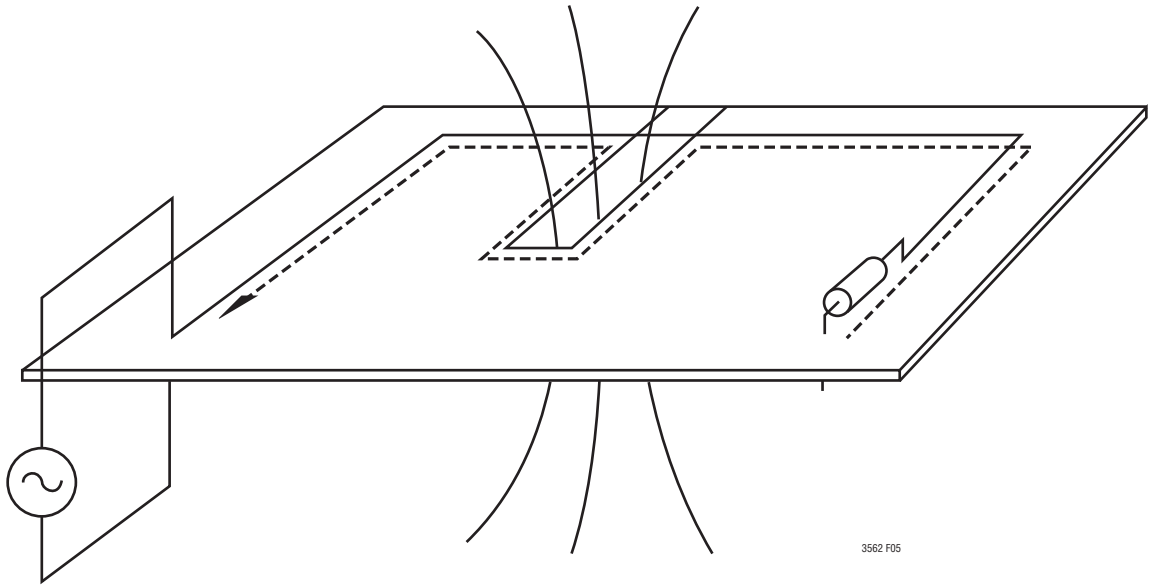
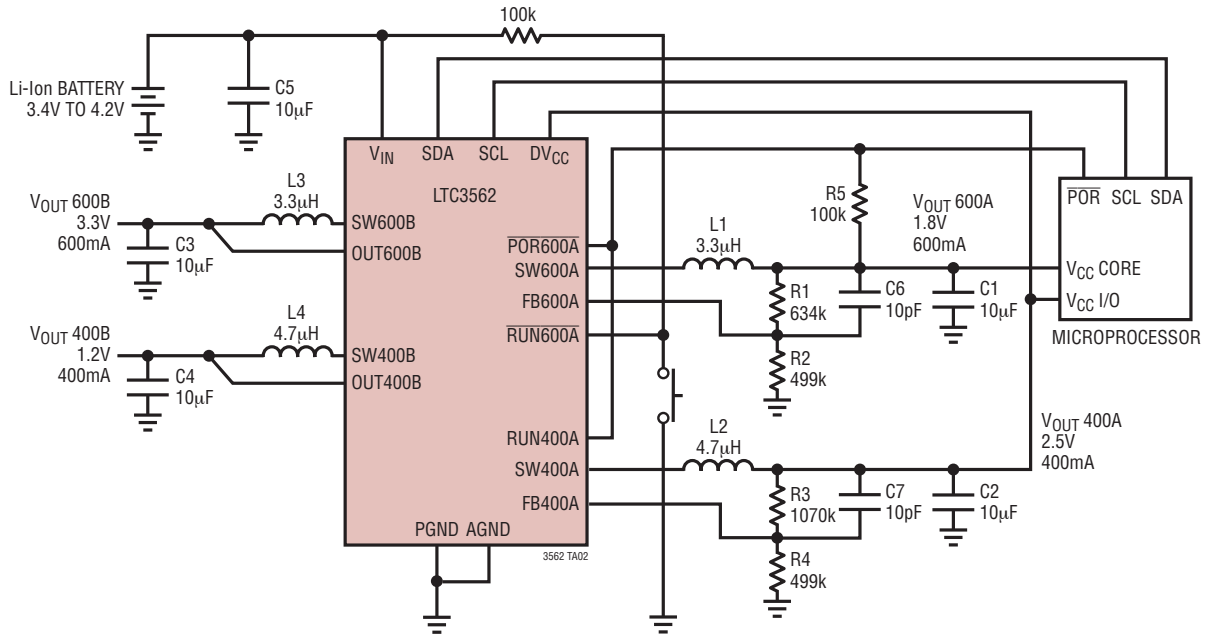


Figure 5. High Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Cause High Voltage and Increased Emissions.

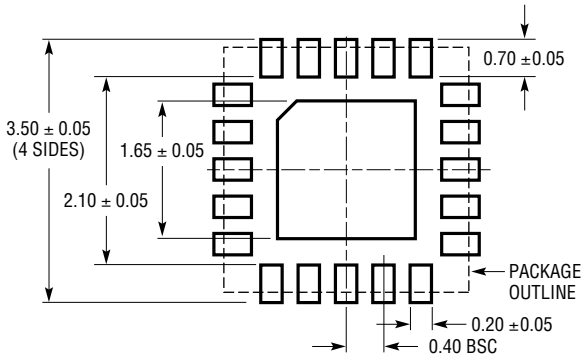
TYPICAL APPLICATION

Quad Step-Down Converter with Push Button Control and Power Sequencing



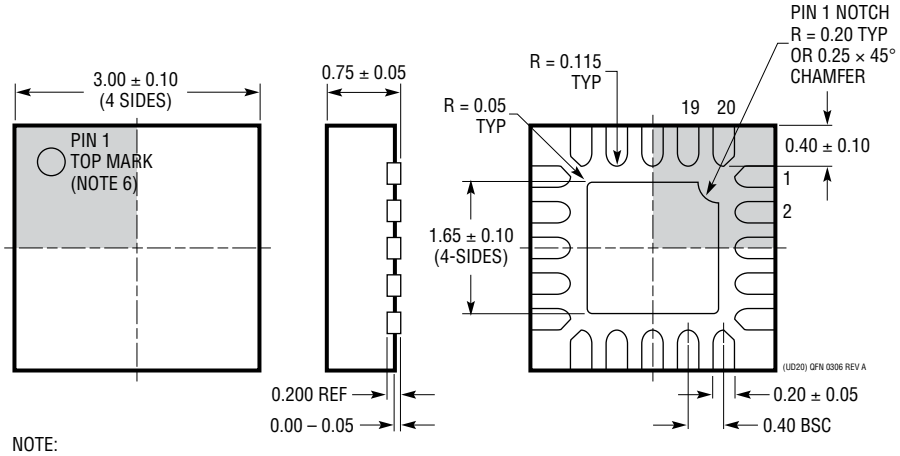
PACKAGE DESCRIPTION

UD Package
20-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1720 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3406/ LTC3406B	600mA I_{OUT}, 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT™ Package
LTC3407/ LTC3407-2	Dual 600mA/800mA I_{OUT}, 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E and DFN Packages
LTC3410/ LTC3410B	300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} < 1µA, SC70 Package
LTC3531/LTC3531-3/ LTC3531-3.3	200mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 1.8V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT and DFN Packages
LTC3532	500mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.4V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, MS10 and DFN Packages
LTC3542	500mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 26µA, I_{SD} < 1µA, 2mm × 2mm DFN Package
LTC3544/LTC3544B	Quad 300mA and 2 × 200mA and 100mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm QFN Package
LTC3547/ LTC3547B	Dual 300mA, 2.25MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, 2mm × 3mm DFN Package
LTC3548/LTC3548-1/ LTC3548-2	Dual 400mA and 800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, MS10E and DFN Packages
LTC3560	800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT Package

ThinSOT is a trademark of Linear Technology Corporation

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