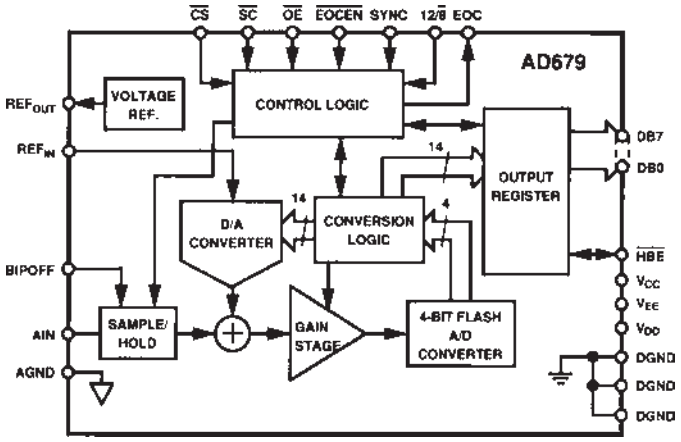
# 14-Bit 128 kSPS Complete Sampling ADC

# AD679

**FEATURES**

**AC and DC Characterized and Specified (K, B, T Grades)**
**128k Conversions per Second**
**1 MHz Full Power Bandwidth**
**500 kHz Full Linear Bandwidth**
**78 dB S/N+D (K, B, T Grades)**
**Twos Complement Data Format (Bipolar Mode)**
**Straight Binary Data Format (Unipolar Mode)**
**10 MΩ Input Impedance**
**8-Bit Bus Interface**
**On-Board Reference and Clock**
**10 V Unipolar or Bipolar Input Range**
**Pin Compatible with AD678 12-Bit, 200 kSPS ADC**
**MIL-STD-883 Compliant Versions Available**

**FUNCTIONAL BLOCK DIAGRAM**




## GENERAL DESCRIPTION

The AD679 is a complete, multipurpose 14-bit monolithic analog-to-digital converter, consisting of a sample-and-hold amplifier (SHA), a microprocessor-compatible bus interface, a voltage reference, and clock generation circuitry.

The AD679 is specified for ac (or dynamic) parameters such as S/N+D ratio, THD, and IMD, which are important in signal processing applications. In addition, the AD679K, B, and T grades are fully specified for dc parameters that are important in measurement applications.

The 14 data bits are accessed in two read operations (8 + 6), with left justification. Data format is straight binary for unipolar mode and twos complement binary for bipolar mode. The input has a full-scale range of 10 V with a full power bandwidth of 1 MHz and a full linear bandwidth of 500 kHz. High input impedance (10 MΩ) allows direct connection to unbuffered sources without signal degradation. Conversions can be initiated either under microprocessor control or by an external clock asynchronous to the system clock.

This product is fabricated on Analog Devices' BiMOS process, combining low power CMOS logic with high precision, low noise bipolar circuits; laser-trimmed thin-film resistors provide high accuracy. The converter utilizes a recursive subranging algorithm that includes error correction and flash converter circuitry to achieve high speed and resolution.

The AD679 operates from +5 V and ±12 V supplies and dissipates 560 mW (typ). The part is available in 28-lead plastic DIP, ceramic DIP, and 44 J-leaded ceramic surface-mount packages.

## PRODUCT HIGHLIGHTS

1. COMPLETE INTEGRATION: The AD679 minimizes external component requirements by combining a high speed sample-and-hold amplifier (SHA), ADC, 5 V reference, clock, and digital interface on a single chip. This provides a fully specified sampling A/D function unattainable with discrete designs.
2. SPECIFICATIONS: The AD679K, B, and T grades provide fully specified and tested ac and dc parameters. The AD679J, A, and S grades are specified and tested for ac parameters; dc accuracy specifications are shown as typicals. DC specifications (such as INL, gain, and offset) are important in control and measurement applications. AC specifications (such as S/N+D ratio, THD, and IMD) are of value in signal processing applications.
3. EASE OF USE: The pinout is designed for easy board layout, and the two-read output provides compatibility with 8-bit buses. Factory trimming eliminates the need for calibration modes or external trimming to achieve rated performance.
4. RELIABILITY: The AD679 utilizes Analog Devices' monolithic BiMOS technology. This ensures long-term reliability compared to multichip and hybrid designs.
5. UPGRADE PATH: The AD679 provides the same pinout as the 12-bit, 200 kSPS AD678 ADC.
6. The AD679 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD679/883B data sheet for detailed specifications.

REV. D



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# AD679–SPECIFICATIONS

## AC SPECIFICATIONS ($T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +12 V ± 5%, $V_{EE}$ = –12 V ± 5%, $V_{DD}$ = +5 V ± 10%, $f_{SAMPLE}$ = 128 kSPS, $f_{IN}$ = 10.009 kHz, unless otherwise noted)[1]

| Parameter | AD679J/A/S Min | AD679J/A/S Typ | AD679J/A/S Max | AD679K/B/T Min | AD679K/B/T Typ | AD679K/B/T Max | Unit |
|---|---|---|---|---|---|---|---|
| SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO[2] | | | | | | | |
| –0.5 dB Input (Referred to –0 dB Input) | 76 | 79 | | 78 | 81 | | dB |
| –20 dB Input (Referred to –20 dB Input) | 58 | 59 | | 60 | 61 | | dB |
| –60 dB Input (Referred to –60 dB Input) | 18 | 19 | | 20 | 21 | | dB |
| TOTAL HARMONIC DISTORTION (THD)[3] | | | | | | | |
| @ 25°C | | –90 | –82 | | –90 | –82 | dB |
| | | 0.003 | 0.006 | | 0.003 | 0.006 | % |
| $T_{MIN}$ to $T_{MAX}$ | | –88 | –82 | | –88 | –82 | dB |
| | | 0.004 | 0.008 | | 0.004 | 0.008 | % |
| PEAK SPURIOUS OR PEAK HARMONIC COMPONENT | | –90 | –82 | | –90 | –82 | dB |
| FULL POWER BANDWIDTH | | 1 | | | 1 | | MHz |
| FULL LINEAR BANDWIDTH | 500 | | | 500 | | | kHz |
| INTERMODULATION DISTORTION (IMD)[4] | | | | | | | |
| 2nd Order Products | | –90 | –82 | | –90 | –82 | dB |
| 3rd Order Products | | –90 | –82 | | –90 | –82 | dB |

NOTES
[1]$f_{IN}$ amplitude = –0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a –0 dB (9.997 V p-p) input signal unless otherwise noted.
[2]See TPC 3 for higher frequencies and other input amplitudes.
[3]See TPCs 1 and 2 for higher frequencies and other input amplitudes.
[4]$f_A$ = 9.08 kHz, $f_B$ = 9.58 kHz, with $f_{SAMPLE}$ 100 kSPS. See Definition of Specifications section.

Specifications subject to change without notice.

## DIGITAL SPECIFICATIONS (All device types $T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +12 V ± 5%, $V_{EE}$ = –12 V ± 5%, $V_{DD}$ = +5 V ± 10%)

| Parameter | | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | $V_{DD}$ | V |
| $V_{IL}$ | Low Level Input Voltage | | 0 | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = 5 V | –10 | +10 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0 V | –10 | +10 | μA |
| $C_{IN}$ | Input Capacitance | | | 10 | pF |
| LOGIC OUTPUTS | | | | | |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = 0.1 mA | 4.0 | | V |
| | | $I_{OH}$ = 0.5 mA | 2.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$ = 1.6 mA | | 0.4 | V |
| $I_{OZ}$ | High Z Leakage Current | $V_{IN}$ = 0 or 5 V | –10 | +10 | μA |
| $C_{OZ}$ | High Z Output Capacitance | | | 10 | pF |

NOTES
[1]$f_{IN}$ amplitude = –0.5 dB (9.44 V p-p) bipolar mode full scale unless otherwise indicated. All measurements referred to a –0 dB (9.997 V p-p) input signal unless otherwise noted.
[2]See TPC 3 for higher frequencies and other input amplitudes.
[3]See TPCs 1 and 2 for higher frequencies and other input amplitudes.
[4]$f_A$ = 9.08 kHz, $f_B$ = 9.58 kHz, with $f_{SAMPLE}$ 100 kSPS. See Definition of Specifications section.

Specifications subject to change without notice.

## DC SPECIFICATIONS ($T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +12 V ± 5%, $V_{EE}$ = –12 V ± 5%, $V_{DD}$ = +5 V ± 10%, unless otherwise noted)

| Parameter | AD679J/A/S Min | AD679J/A/S Typ | AD679J/A/S Max | AD679K/B/T Min | AD679K/B/T Typ | AD679K/B/T Max | Unit |
|---|---|---|---|---|---|---|---|
| TEMPERATURE RANGE | | | | | | | |
| J, K Grades | 0 | | 70 | 0 | | 70 | °C |
| A, B Grades | –40 | | +85 | –40 | | +85 | °C |
| S, T Grades | –55 | | +125 | –55 | | +125 | °C |
| ACCURACY | | | | | | | |
| Resolution | **14** | | | **14** | | | Bits |
| Integral Nonlinearity (INL) | | ±2 | | | ±1 | **±2.5** | LSB |
| Differential Nonlinearity (DNL) | **14** | | | **14** | | | Bits |
| Unipolar Zero Error[1] (@ 25°C) | | 0.08 | | | 0.05 | **0.07** | % FSR[2] |
| Bipolar Zero Error[1] (@ 25°C) | | 0.08 | | | 0.05 | **0.07** | % FSR |
| Gain Error[1, 3] (@ 25°C) | | 0.12 | | | 0.09 | **0.11** | % FSR |
| Temperature Drift | | | | | | | |
| Unipolar Zero[4] | | | | | | | |
| J, K Grades | | 0.04 | | | 0.04 | **0.05** | % FSR |
| A, B Grades | | 0.05 | | | 0.05 | **0.07** | % FSR |
| S, T Grades | | 0.09 | | | 0.09 | **0.10** | % FSR |
| Bipolar Zero[4] | | | | | | | |
| J, K Grades | | 0.02 | | | 0.02 | **0.04** | % FSR |
| A, B Grades | | 0.04 | | | 0.04 | **0.05** | % FSR |
| S, T Grades | | 0.08 | | | 0.08 | **0.09** | % FSR |
| Gain[4] | | | | | | | |
| J, K Grades | | 0.09 | | | 0.09 | **0.11** | % FSR |
| A, B Grades | | 0.10 | | | 0.10 | **0.16** | % FSR |
| S, T Grades | | 0.20 | | | 0.20 | **0.25** | % FSR |
| Gain[5] | | | | | | | |
| J, K Grades | | 0.04 | | | 0.04 | **0.05** | % FSR |
| A, B Grades | | 0.05 | | | 0.05 | **0.07** | % FSR |
| S, T Grades | | 0.09 | | | 0.09 | **0.10** | % FSR |
| ANALOG INPUT | | | | | | | |
| Input Ranges | | | | | | | |
| Unipolar Mode | **0** | | **+10** | **0** | | **+10** | V |
| Bipolar Mode | **–5** | | **+5** | **–5** | | **+5** | V |
| Input Resistance | | 10 | | | 10 | | MΩ |
| Input Capacitance | | 10 | | | 10 | | pF |
| Input Settling Time | | | 1.5 | | | 1.5 | µs |
| Aperture Delay | | 10 | | | 10 | | ns |
| Aperture Jitter | | 150 | | | 150 | | ps |
| INTERNAL VOLTAGE REFERENCE | | | | | | | |
| Output Voltage[6] | **4.98** | | **5.02** | **4.98** | | **5.02** | V |
| External Load | | | | | | | |
| Unipolar Mode | | | **1.5** | | | **1.5** | mA |
| Bipolar Mode | | | **0.5** | | | **0.5** | mA |
| POWER SUPPLIES | | | | | | | |
| Power Supply Rejection | | | | | | | |
| $V_{CC}$ = +12 V ± 5% | | ±6 | | | | **±6** | LSB |
| $V_{EE}$ = –12 V ± 5% | | ±6 | | | | **±6** | LSB |
| $V_{DD}$ = +5 V ± 10% | | ±6 | | | | **±6** | LSB |
| Operating Current | | | | | | | |
| $I_{CC}$ | | 18 | **20** | | 18 | **20** | mA |
| $I_{EE}$ | | 25 | **34** | | 25 | **34** | mA |
| $I_{DD}$ | | 8 | **12** | | 8 | **12** | mA |
| Power Consumption | | 560 | 745 | | 560 | 745 | mW |

NOTES

[1]Adjustable to zero. See Figures 5 and 6.

[2]% FSR = percent of full-scale range.

[3]Includes internal voltage reference error.

[4]Includes internal voltage reference drift.

[5]Excludes internal voltage reference drift.

[6]With maximum external load applied.

Specifications shown in **boldface** are tested on all devices at final electrical test with worst case supply voltages at $T_{MIN}$, 25°C and $T_{MAX}$. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested.

Specifications subject to change without notice.

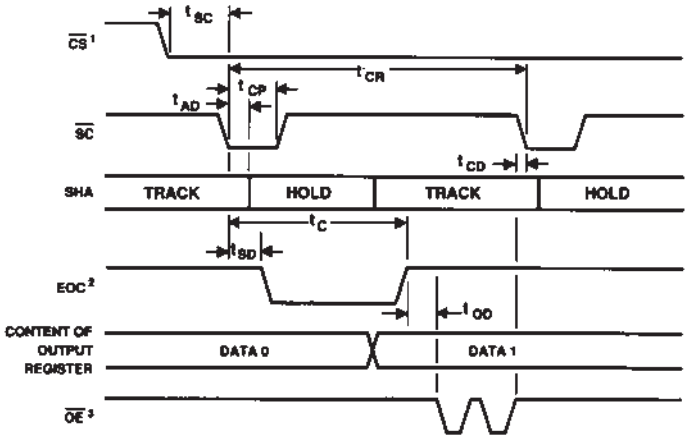
## TIMING SPECIFICATIONS

(All device types $T_{MIN}$ to $T_{MAX}$, $V_{CC}$ = +12 V ± 5%, $V_{EE}$ = –12 V ± 5%, $V_{DD}$ = +5 V ± 10%)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $\overline{SC}$ Delay | $t_{SC}$ | 50 | | ns |
| Conversion Time | $t_C$ | | 6.3 | µs |
| Conversion Rate[1] | $t_{CR}$ | | 7.8 | µs |
| Convert Pulse Width | $t_{CP}$ | 0.097 | 3.0 | µs |
| Aperture Delay | $t_{AD}$ | 5 | 20 | ns |
| Status Delay | $t_{SD}$ | 0 | 400 | ns |
| Access Time[2, 3] | $t_{BA}$ | 10 | 100 | ns |
| | | 10 | 57[4] | ns |
| Float Delay[5] | $t_{FD}$ | 10 | 80 | ns |
| Output Delay | $t_{OD}$ | | 0 | ns |
| Format Setup | $t_{FS}$ | 100 | | ns |
| $\overline{OE}$ Delay | $t_{OE}$ | 20 | | ns |
| Read Pulse Width | $t_{RP}$ | 195 | | ns |
| Conversion Delay | $t_{CD}$ | 400 | | ns |
| $\overline{EOCEN}$ Delay | $t_{EO}$ | 50 | | ns |

NOTES
[1]Includes acquisition time.
[2]Measured from the falling edge of $\overline{OE}$/$\overline{EOCEN}$ (0.8 V) to the time at which the data lines/EOC cross 2.0 V or 0.8 V. See Figure 4.
[3]$C_{OUT}$ = 100 pF.
[4]$C_{OUT}$ = 50 pF.
[5]Measured from the rising edge of $\overline{OE}$/$\overline{EOCEN}$ (2.0 V) to the time at which the output voltage changes by 0.5. See Figure 4; $C_{OUT}$ = 10 pF.

Specifications subject to change without notice.




NOTES
[1]IN ASYNCHRONOUS MODE, STATE OF $\overline{CS}$ DOES NOT AFFECT OPERATION. SEE THE START CONVERSION TRUTH TABLE FOR DETAILS.
[2]$\overline{EOCEN}$ = LOW (SEE FIGURE 3). IN SYNCHRONOUS MODE, EOC IS A THREE-STATE OUTPUT. IN ASYNCHRONOUS MODE, EOC IS AN OPEN DRAIN OUTPUT.
[3]DATA SHOULD NOT BE ENABLED DURING A CONVERSION.

*Figure 1. Conversion Timing*

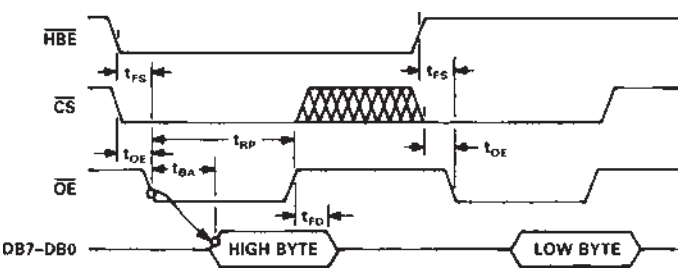
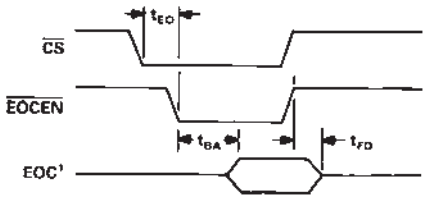



*Figure 2. Output Timing*




NOTE
[1]EOC IS A THREE-STATE OUTPUT IN SYNCHRONOUS MODE AND AN OPEN DRAIN OUTPUT IN ASYNCHRONOUS. ACCESS ($t_{BA}$) AND FLOAT ($t_{FD}$) TIMING SPECIFICATIONS DO NOT APPLY IN ASYNCHRONOUS MODE WHERE THEY ARE A FUNCTION OF THE TIME CONSTANT FORMED BY THE 10pF OUTPUT CAPACITANCE AND THE PULL-UP RESISTOR.

*Figure 3. EOC Timing*

| TEST | $V_{CP}$ | $C_{OUT}$ |
|---|---|---|
| ACCESS TIME HIGH Z TO LOGIC LOW | 5V | 100pF |
| FLOAT TIME LOGIC HIGH TO HIGH Z | 0V | 10pF |
| ACCESS TIME HIGH Z TO LOGIC HIGH | 0V | 100pF |
| FLOAT TIME LOGIC LOW TO HIGH Z | 5V | 10pF |

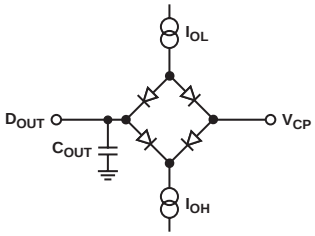



*Figure 4. Load Circuit for Bus Timing Specifications*

**ABSOLUTE MAXIMUM RATINGS**[1]

| Specification | With Respect To | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | AGND | –0.3 | +18 | V |
| $V_{EE}$ | AGND | –18 | +0.3 | V |
| $V_{CC}$[2] | $V_{EE}$ | –0.3 | +26.4 | V |
| $V_{DD}$ | DGND | 0 | +7 | V |
| AGND | DGND | –1 | +1 | V |
| AIN, $REF_{IN}$ | AGND | $V_{EE}$ | $V_{CC}$ | V |
| Digital Inputs | DGND | –0.5 | +7 | V |
| Digital Outputs | DGND | –0.5 | $V_{DD}$ + 0.3 | V |
| Max Junction Temperature | | | 175 | °C |

| Specification | With Respect To | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | | | | |
| J and K Grades | | 0 | 70 | °C |
| A and B Grades | | –40 | +85 | °C |
| S and T Grades | | –55 | +125 | °C |
| Storage Temperature | | –65 | +150 | °C |
| Lead Temperature (10 sec max) | | | 300 | °C |

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The AD679 is not designed to operate from ±15 V supplies.

**ORDERING GUIDE**[1]

| Model | Package | Temperature Range | Tested and Specified | Package Option[2] |
|---|---|---|---|---|
| AD679JN | 28-Pin Plastic DIP | 0°C to +70°C | AC | N-28 |
| AD679KN | 28-Pin Plastic DIP | 0°C to +70°C | AC + DC | N-28 |
| AD679JD | 28-Pin Ceramic DIP | 0°C to +70°C | AC | D-28 |
| AD679KD | 28-Pin Ceramic DIP | 0°C to +70°C | AC + DC | D-28 |
| AD679AD | 28-Pin Ceramic DIP | –40°C to +85°C | AC | D-28 |
| AD679BD | 28-Pin Ceramic DIP | –40°C to +85°C | AC + DC | D-28 |
| AD679SD | 28-Pin Ceramic DIP | –55°C to +125°C | AC | D-28 |
| AD679TD | 28-Pin Ceramic DIP | –55°C to +125°C | AC + DC | D-28 |
| AD679AJ | 44-Lead Ceramic JLCC | –40°C to +85°C | AC | J-44 |
| AD679BJ | 44-Lead Ceramic JLCC | –40°C to +85°C | AC + DC | J-44 |
| AD679SD/883B[3] | | | | |

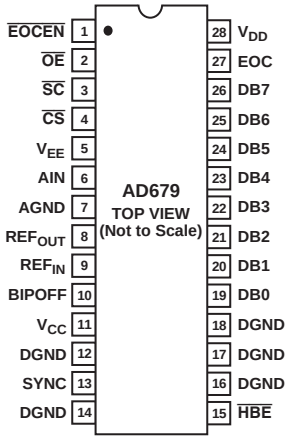
NOTES
[1]For parallel read (14-bits) interface to 16-bit buses, see AD779.
[2]N = Plastic DIP; D = Ceramic DIP; J = J-Leaded Ceramic Chip Carrier.
[3]For details, grade, and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or the current AD679/883B data sheet.

**CAUTION**

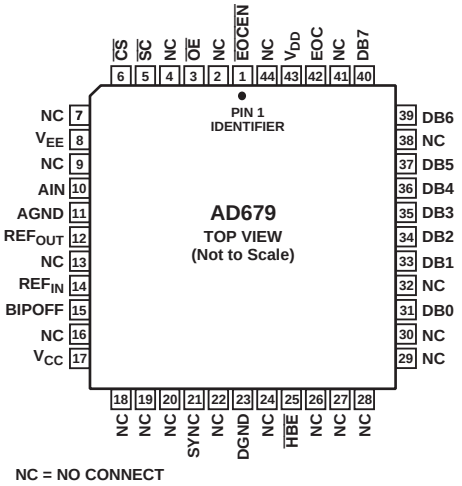
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD679 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS

**DIP Package**




**JLCC Package**




NC = NO CONNECT

## PIN FUNCTION DESCRIPTIONS

| Mnemonic | 28-Lead DIP Pin No. | 44-Lead JLCC Pin No. | Type | Name and Function |
|---|---|---|---|---|
| AGND | 7 | 11 | P | Analog Ground. This is the ground return for AIN only. |
| AIN | 6 | 10 | AI | Analog Signal Input. |
| BIPOFF | 10 | 15 | AI | Bipolar Offset. Connect to AGND for +10 V input unipolar mode and straight binary output coding. Connect to $REF_{OUT}$ for ±5 V input bipolar mode and twos complement binary output coding. |
| $\overline{CS}$ | 4 | 6 | DI | Chip Select. Active LOW. |
| DGND | 12, 14 | 23 | P | Digital Ground. |
| DB7–DB0 | 26–19 | 40, 39, 37, 36, 35, 34, 33, 31 | DO | Data Bits. These pins provide all 14 bits in two bytes (8 + 6 bits). Active HIGH. |
| EOC | 27 | 42 | DO | End-of-Convert. EOC goes LOW when a conversion starts and goes HIGH when the conversion finishes. In asynchronous mode, EOC is an open-drain output and requires an external 3 kΩ pull-up resistor. See $\overline{EOCEN}$ and SYNC pins for information on EOC gating. |
| $\overline{EOCEN}$ | 1 | 1 | DI | End-of-Convert Enable. Enables EOC pin. Active LOW. |
| $\overline{HBE}$ | 15 | 25 | DI | High Byte Enable. If LOW, output contains high byte. If HIGH, output contains low byte (corresponding to the most recently read high byte). |
| $\overline{OE}$ with $REF_{IN}$ | 2 | 3 | DI | Output Enable. A down-going transition on $\overline{OE}$ enables DB7 to DB0. Gated $\overline{CS}$. Active LOW. |
| $REF_{IN}$ | 9 | 14 | AI | Reference Input. 5 V input gives 10 V full-scale range. |
| $REF_{OUT}$ | 8 | 12 | AO | 5 V Reference Output. Tied to $REF_{IN}$ for normal operation. |
| $\overline{SC}$ | 3 | 5 | DI | Start Convert. Active LOW. See SYNC pin for gating. |
| SYNC | 13 | 21 | DI | SYNC Control. If tied to $V_{DD}$ (synchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are gated by $\overline{CS}$. If tied to DGND (asynchronous mode), $\overline{SC}$ and $\overline{EOCEN}$ are independent of $\overline{CS}$, and EOC is an open-drain output. EOC requires an external 3 kΩ pull-up resistor in asynchronous mode. |
| $V_{CC}$ | 11 | 17 | P | 12 V Analog Power. |
| $V_{EE}$ | 5 | 8 | P | –12 V Analog Power. |
| $V_{DD}$ | 28 | 43 | P | 5 V Digital Power. |
| — | 16 | | U | Tie to DGND. |
| — | 17–18 | 2, 4, 7, 9, 13, 16, 18, 19, 20, 22, 24, 26, 27, 28, 29, 30, 32, 38, 41, 44 | U | These pins are unused and should be connected to DGND or $V_{DD}$. |

Type: AI = Analog Input. AO = Analog Output. DI = Digital Input (TTL and 5 V CMOS compatible). DO = Digital Output (TTL and 5 V CMOS compatible). All DO pins are three-state drivers. P = Power. U = Unused.

## DEFINITIONS OF SPECIFICATIONS

**Nyquist Frequency**
An implication of the Nyquist sampling theorem, the Nyquist frequency of a converter is the input frequency that is one-half the sampling frequency of the converter.

**Signal-to-Noise and Distortion (S/N+D) Ratio**
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics above the Nyquist frequency, the aliased component is used.

**Peak Spurious or Peak Harmonic Component**
The peak spurious or peak harmonic component is the largest spectral component excluding the input signal and dc. This value is expressed in decibels relative to the rms value of a full-scale input signal.

**Intermodulation Distortion (IMD)**
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n) at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3…. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb) and the third order terms are (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is –0.5 dB from full-scale (9.44 V p-p). The IMD products are normalized to a 0 dB input signal.

**Bandwidth**
The full-power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-and-hold amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than –0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

The AD679 has been designed to optimize input bandwidth, allowing it to undersample input signals with frequencies significantly above the converter's Nyquist frequency.

**Aperture Delay**
Aperture delay is a measure of the SHA's performance and is measured from the falling edge of start convert ($\overline{SC}$) to when the input signal is held for conversion. In synchronous mode, chip select ($\overline{CS}$) should be LOW before $\overline{SC}$ to minimize aperture delay.

**Aperture Jitter**
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

**Input Setting Time**
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

**Differential Nonlinearity (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. Differential linearity is the deviation from this ideal value. It is often specified in terms of resolution for which no missing codes (NMC) are guaranteed.

**Integral Nonlinearity (INL)**
The ideal transfer function for a linear ADC is a straight line drawn between zero and full scale. The point used as zero occcurs 1/2 LSB before the first code transition. Full scale is defined as a level 1 1/2 LSB beyond the last code transition. Integral linearity error is the worst case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

Note that the linearity error is not user adjustable.

**Power Supply Rejection**
Variations in power supply will affect the full-scale transition, but not the converter's linearity. Power Supply Rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

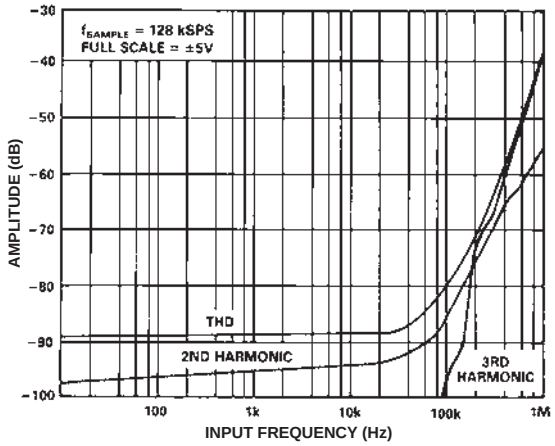
**Temperature Drift**
This is the maximum change in the parameter from the initial value (@ 25°C) to the value at $T_{MIN}$ or $T_{MAX}$.

**Unipolar Zero Error**
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. Unipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

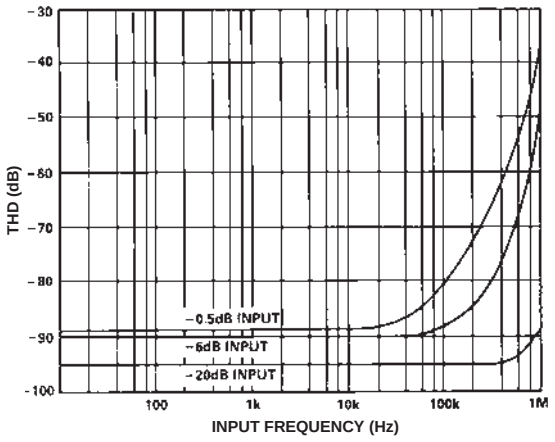
**Bipolar Zero Error**
In the bipolar mode, the major carry transition (11 1111 1111 1111 to 00 0000 0000 0000 ) should occur at an analog value 1/2 LSB below analog ground. Bipolar zero error is the deviation of the actual transition from that point. This error can be adjusted as discussed in the Input Connections and Calibration section.

**Gain Error**
The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale (9.9991 V for a 0 V to 10 V range, 4.9991 V for a ±5 V range). The gain error is the deviation of the actual level at the last transition from the ideal level with the zero error trimmed out. This error can be adjusted as shown in the Input Connections and Calibration section.

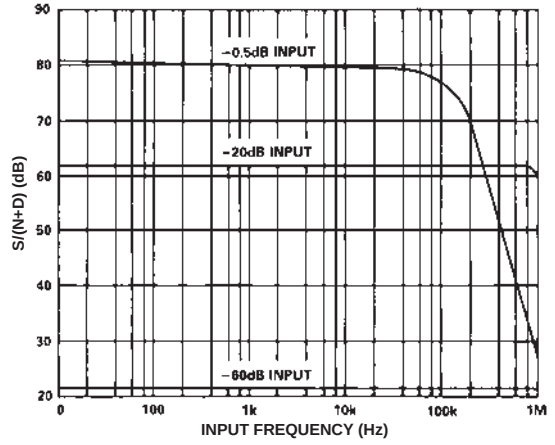
# AD679–Typical Performance Characteristics



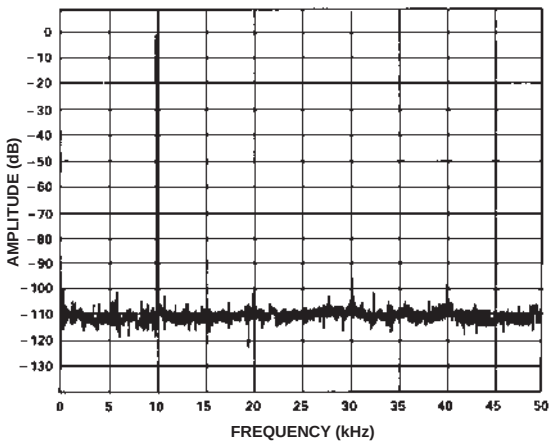

*TPC 1. Harmonic Distortion vs. Input Frequency (–0.5 dB Input)*



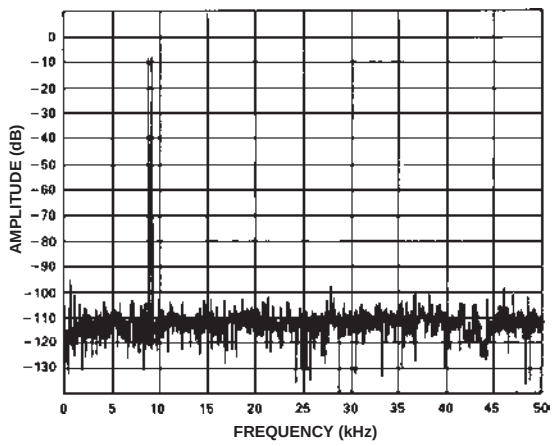

*TPC 2. Total Harmonic Distortion vs. Input Frequency and Amplitude*



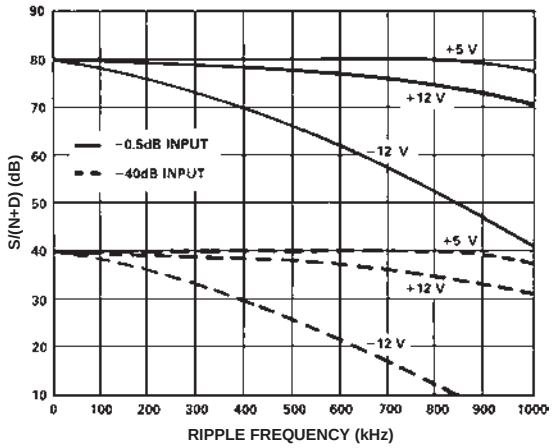

*TPC 3. S/(N+D) vs. Input Frequency and Amplitude*




*TPC 4. 5-Plot Averaged 2048 Point FFT at 128 kSPS, $f_{IN}$ = 10.009 kHz*




*TPC 5. Nonaveraged IMD Plot for $f_{IN}$ = 9.08 kHz ($f_a$), 9.58 kHz ($f_b$) at 128 kSPS*




*TPC 6. Power Supply Rejection ($f_{IN}$ = 10 kHz, $f_{SAMPLE}$ = 128 kSPS, $V_{RIPPLE}$ = 0.1 V p-p)*

## CONVERSION CONTROL

In synchronous mode (SYNC = HIGH), both chip select ($\overline{CS}$) and start convert ($\overline{SC}$) must be brought LOW to start a conversion. $\overline{CS}$ should be LOW $t_{SC}$ before $\overline{SC}$ is brought LOW. In asynchronous mode (SYNC = LOW), a conversion is started by bringing $\overline{SC}$ low, regardless of the state of $\overline{CS}$.

Before a conversion is started, end-of-convert (EOC) is HIGH and the sample-and-hold is in track mode. After a conversion is started, the sample-and-hold goes into hold mode and EOC goes LOW, signifying that a conversion is in progress. During the conversion, the sample-and-hold will go back into track mode and start acquiring the next sample.

In track mode, the sample-and-hold will settle to ±0.003% (14 bits) in 1.5 µs maximum. The acquisition time does not affect the throughput rate as the AD679 goes back into track mode more than 2 µs before the next conversion. In multichannel systems, the input channel can be switched as soon as EOC goes LOW.

Bringing $\overline{OE}$ LOW $t_{OE}$ after $\overline{CS}$ goes LOW makes the output register contents available on the output data bits (DB7–DB0). A period of time, $t_{CD}$, is required after $\overline{OE}$ is brought HIGH before the next SC instruction is issued.

If $\overline{SC}$ is held LOW, conversion accuracy may deteriorate. For this reason, $\overline{SC}$ should not be held low in an attempt to operate in a continuously converting mode.

**Table I. Start Conversion Truth Table**

| | Inputs | | | |
|---|---|---|---|---|
| | SYNC | $\overline{CS}$ | $\overline{SC}$ | Status |
| Synchronous Mode | 1 | 1 | X | No Conversion |
| | 1 | 0 | ↓ | Start Conversion |
| | 1 | ↓ | 0 | Start Conversion (Not Recommended) |
| | 1 | 0 | 0 | Continuous Conversion (Not Recommended) |
| Asynchronous Mode | 0 | X | 1 | No Conversion |
| | 0 | X | ↓ | Start Conversion |
| | 0 | X | 0 | Continuous Conversion (Not Recommended) |

1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
↓ = HIGH to LOW transition. Must stay low for t = $t_{CP}$.

**Table II. 14-Bit Mode Coding Format (1 LSB = 0.61 mV)**

| Unipolar Coding (Straight Binary) | | Bipolar Coding (Twos Complement) | |
|---|---|---|---|
| $V_{IN}$* | Output Code | $V_{IN}$* (V) | Output Code |
| 0.00000 V | 000 . . . 0 | –5.00000 | 100 . . . 0 |
| 5.00000 V | 100 . . . 0 | –0.00061 | 111 . . . 1 |
| 9.99939 V | 111 . . . 1 | 0.00000 | 000 . . . 0 |
| | | +2.50000 | 010 . . . 0 |
| | | +4.99939 | 011 . . . 1 |

*Code center.

## END-OF-CONVERT

In asynchronous mode, end-of-convert (EOC) is an open-drain output (requiring a minimum 3 kΩ pull-up resistor) enabled by end-of-convert enable ($\overline{EOCEN}$). In synchronous mode, EOC is a three-state output that is enabled by $\overline{EOCEN}$ and $\overline{CS}$. See Table III. Access ($t_{BA}$) and float ($t_{FD}$) timing specifications do not apply in asynchronous mode where they are a function of the time constant formed by the external load capacitance and the pull-up resistor.

## OUTPUT ENABLE OPERATION

The data bits (DB7–DB0) are three-state outputs that are enabled by chip select ($\overline{CS}$) and output enable ($\overline{OE}$). $\overline{CS}$ should be LOW $t_{OE}$ before $\overline{OE}$ is brought LOW.

When EOC goes HIGH, the conversion is completed and the output data may be read. The output is read in two steps as a 16-bit word, with the high byte read first, followed by the low byte. High byte enable ($\overline{HBE}$) controls the output sequence. The 14-bit result is left justified within the 16-bit field.

In unipolar mode (BIPOFF tied to AGND), the output coding is straight binary. In bipolar mode (BIPOFF tied to $REF_{OUT}$), output coding is twos complement binary.

## POWER-UP

The AD679 typically requires 10 µs after power-up to reset internal logic.

**Table III. Conversion Status Truth Table**

| | Inputs | | | Output | |
|---|---|---|---|---|---|
| | SYNC | $\overline{CS}$ | $\overline{EOCEN}$ | EOC | Status |
| Synchronous Mode | 1 | 0 | 0 | 0 | Converting |
| | 1 | 0 | 0 | 1 | Not Converting |
| | 1 | 1 | X | High Z | Either |
| | 1 | X | 1 | High Z | Either |
| Asynchronous Mode* | 0 | X | 0 | 0 | Converting |
| | 0 | X | 0 | High Z | Not Converting |
| | 0 | X | 1 | High Z | Either |

1 = HIGH voltage level.
0 = LOW voltage level.
X = Don't care.
*EOC requires a pull-up resistor in asynchronous mode.

**Table IV. Output Enable Truth Table**

| | Inputs | | Outputs |
|---|---|---|---|
| | $\overline{HBE}$ | ($\overline{CS}$ U $\overline{OE}$) | DB7 . . . DB0 |
| | X | 1 | ← High Z → |
| Unipolar or Bipolar | 0 | 0 | a b c d e f g h |
| | 1 | 0 | i j k l m n 0 0 |

1 = HIGH voltage level. a = MSB.
0 = LOW voltage level. n = LSB.
X = Don't care.
U = Logical OR.
Data coding is binary for unipolar mode and twos complement binary for bipolar mode.

## INPUT CONNECTIONS AND CALIBRATION

The high (10 MΩ) input impedance of the AD679 eases the task of interfacing to high source impedances or multiplexer channel-to-channel mismatches of up to 300 Ω. The 10 V p-p full-scale input range accepts the majority of signal voltages without the need for voltage divider networks that could deteriorate the accuracy of the ADC.

The AD679 is factory trimmed to minimize offset, gain, and linearity errors. In unipolar mode, the only external component that is required is a 50 Ω ±1% resistor. Two resistors are required in bipolar mode. If offset and gain are not critical (as in some ac applications), even these components can be eliminated.

In some applications, offset and gain errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

### Bipolar Range Inputs

The connections for the bipolar mode are shown in Figure 5. In this mode, data output coding is twos complement binary. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

Either or both of the trim pots can be replaced with 50 Ω ±1% fixed resistors if the AD679 accuracy limits are sufficient for application. If the pins are shorted together, the additional offset and gain error is approximately 80 LSB.

To trim bipolar zero to its nominal value, apply a signal 1/2 LSB below midrange (–0.305 mV for a ±5 V range) and adjust R1 until the major carry transition is located (11 1111 1111 1111 to 00 0000 0000 0000). To trim the gain, apply a signal 1 1/2 LSB below full scale (+4.9991 V for a ±5 V range) and adjust R2 to give the last positive transition (01 1111 1111 1110 to 01 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single pass calibration can be done by substituting a bipolar offset trim (error at minus full scale) for the bipolar zero trim (error at midscale) using the same circuit. First, apply a signal 1/2 LSB above minus full scale (–4.9997 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (10 0000 0000 0000 to 10 000 000 0001). Then perform the gain error trim as outlined above.

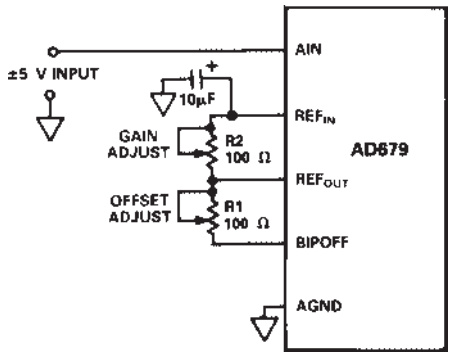



*Figure 5. Bipolar Input Connections with Gain and Offset Trims*

### Unipolar Range Inputs

Offset and gain errors can be trimmed out by using the configuration shown in Figure 6. This circuit allows approximately ±25 mV of offset trim range (±40 LSB) and ±0.5% of gain trim range (±80 LSB).

The nominal offset is 1/2 LSB so that the analog range that corresponds to each code is centered in the middle of that code (halfway between the transitions to the codes above and below it). Thus the first transition (from 00 0000 0000 0000 to 00 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (0.305 mV above ground for a 10 V range). To trim unipolar zero to this nominal value, apply a 0.305 mV signal to AIN and adjust R1 until the first transition is located.

The gain trim is done by adjusting R2. If the nominal value is required, apply a signal 1 1/2 LSB below full scale (9.9997 V for a 10 V range) and adjust R2 until the last transition is located (11 1111 1111 1110 to 11 1111 1111 1111).

If offset adjustment is not required, BIPOFF should be connected directly to AGND. If gain adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If $REF_{OUT}$ is connected directly to $REF_{IN}$, the additional gain error is approximately 1%.

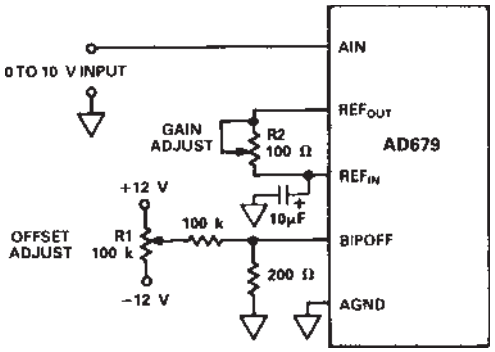



*Figure 6. Unipolar Input Connections with Gain and Offset Trims*

## REFERENCE DECOUPLING

It is recommended that a 10 µF tantalum capacitor be connected between $REF_{IN}$ (Pin 9) and ground. This has the effect of improving the S/N+D ratio through filtering possible broadband noise contributions from the voltage reference.

## BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 1 LSB at the 14-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog

and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

The AD679 incorporates several features to help the user's layout. Analog pins ($V_{EE}$, AIN, AGND, $REF_{OUT}$, $REF_{IN}$, BIPOFF, $V_{CC}$) are adjacent to help isolate analog from digital signals. In addition, the 10 MΩ input impedance of AIN minimizes input trace impedance errors. Finally, ground currents have been minimized by careful circuit architecture. Current through AGND is 200 μA, with no code dependent variation. The current through DGND is dominated by the return current for DB7–DB0 and EOC.

**SUPPLY DECOUPLING**

The AD679 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes that can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and analog ground. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor provides adequate decoupling.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD679, associated analog input circuitry, and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD679 isolates large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

**GROUNDING**

If a single AD679 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND, keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD679. If multiple AD679s are used or if the AD679 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops, which inductively couple noise and allow digital currents to flow through the analog system.

**USE OF EXTERNAL VOLTAGE REFERENCE**

The AD679 features an on-chip voltage reference. For improved gain accuracy over temperature, a high performance external voltage reference may be used in place of the on-chip reference.

The AD586 and AD588 are popular references appropriate for use with high resolution converters. The AD586 is a low cost reference that utilizes a buried Zener architecture to provide low noise and drift. The AD588 is a higher performance reference that uses a proprietary implanted buried Zener diode in conjunction with laser-trimmed thin-film resistors for low offset and low drift.

Figure 7 shows the use of the AD586 with the AD679 in a bipolar input mode. Over the 0°C to 70°C range, the AD586 L-grade exhibits less than a 2.25 mV output change from its initial value at 25°C. $REF_{IN}$ (Pin 9) scales its input by a factor of two; thus, this change becomes effectively 4.5 mV. When applied to the AD679, this results in a total gain drift of 0.09% FSR, which is an improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction capacitor, $C_N$, has been shown.

This capacitor reduces the broadband noise of the AD586 output, thereby optimizing the overall ac and dc performance of the AD679.

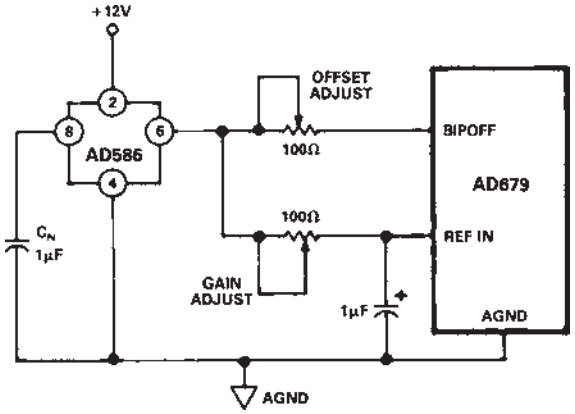



*Figure 7. Bipolar Input with Gain and Offset Trims*

Figure 8 shows the AD679 in unipolar input mode with the AD588 reference. The AD588 output is accurate to 0.65 mV from its value at 25°C over the 0°C to 70°C range. This results in a 0.06% FSR total gain drift for the AD679, a substantial improvement over the on-chip reference performance of 0.11% FSR. A noise-reduction network on Pins 4, 6, and 7 has been shown. The 1 μF capacitors form low-pass filters with the internal resistance of the AD588 Zener and amplifier cells and external resistance. This reduces the high frequency (to 1 MHz) noise of the AD588, providing optimum ac and dc performance of the AD679.

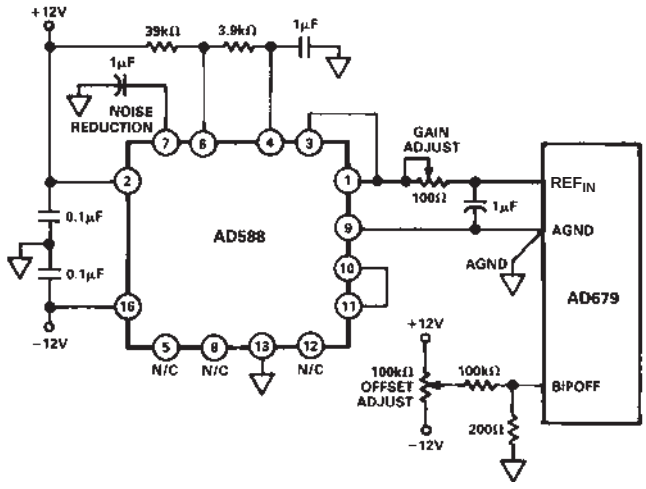



*Figure 8. Unipolar Input with Gain and Offset Trims*

## INTERFACING THE AD679 TO MICROPROCESSORS

The I/O capabilities of the AD679 allow direct interfacing to general-purpose and DSP microprocessor buses. The asynchronous conversion control feature allows complete flexibility and control with minimal external hardware.

The following examples illustrate typical AD679 interface configurations.

### AD679 to TMS320C25

In Figure 9, the AD679 is mapped into the TMS320C25 I/O space. AD679 conversions are initiated by issuing an OUT instruction to Port 1. EOC status and the conversion result are read in with an IN instruction to Port 1. A single wait state is inserted by generating the processor READY input from $\overline{IS}$, Port 1, and $\overline{MSC}$. Address line A0 provides $\overline{HBE}$ decoding to select between the high and low bytes of data. This configuration supports processor clock speeds of 20 MHz and is capable of supporting processor clock speeds of 40 MHz if a NOP instruction follows each AD679 read instruction.

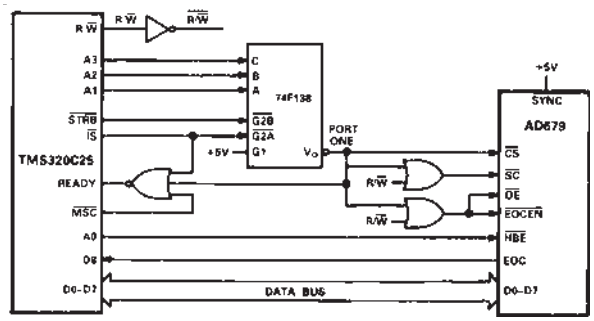



*Figure 9. AD679 to TMS320C25 Interface*

### AD679 to 80186

Figure 10 shows the AD679 interfaced to the 80186 microprocessor. This interface allows the 80186's built-in DMA controller to transfer the AD679 output into a RAM based FIFO buffer of any length, with no microprocessor intervention.

In this application the AD679 is configured in the asynchronous mode, which allows conversions to be initiated by an external trigger source independent of the microprocessor clock. After each conversion, the AD679 EOC signal generates a DMA request to Channel 1 (DRQ1). The subsequent DMA READ sequences the high and low byte AD679 data and resets the interrupt latch. The system designer must assign a sufficient priority to the DMA channel to ensure that the DMA request is serviced before the next conversion is completed. This configuration can be used with 6 MHz and 8 MHz 80186 processors.

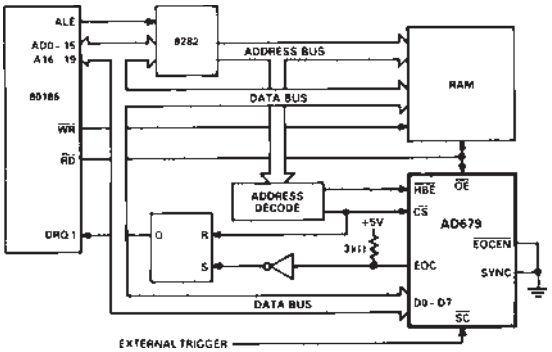



*Figure 10. AD679 to 80186 DMA Interface*

### AD679 to Analog Devices ADSP-2101

Figure 11 demonstrates the AD679 interfaced to an ADSP-2101. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD679 interface with one wait state.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD679 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2101 immediately asserts its FO pin LOW. In the following cycle, the processor starts a data memory read by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter, and the high byte of the conversion result is read over the data bus. The read operation is extended with one wait state and thus started and completed within two processor cycles (160 ns). Next, the ADSP-2101 asserts its FO HIGH. This allows the processor to start reading the lower byte of data. This read operation executes in a similar manner to the first and is completed during the next 160 ns.

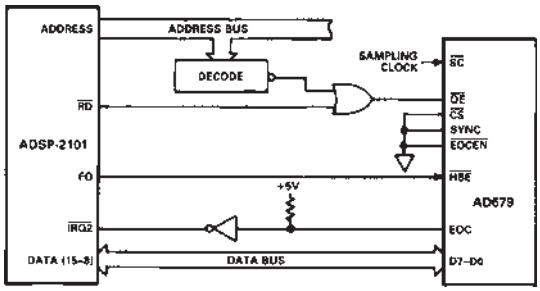



*Figure 11. AD679 to ADSP-2101 Interface*

**AD679 to Analog Devices ADSP-2100A**

Figure 12 demonstrates the AD679 interfaced to an ADSP-2100A. With a clock frequency of 12.5 MHz, and instruction execution in one 80 ns cycle, the digital signal processor supports the AD679 data memory interface with three hardware wait states.

The converter is configured to run asynchronously using a sampling clock. The EOC output of the AD679 gets asserted at the end of each conversion and causes an interrupt. Upon interrupt, the ADSP-2100A immediately executes a data memory write instruction, which asserts $\overline{HBE}$. In the following cycle, the processor starts a data memory read (high byte read) by providing an address on the DMA bus. The decoded address generates $\overline{OE}$ for the converter. $\overline{OE}$, together with logic and latch, is used to force the ADSP-2100A into a one cycle wait state by generating DMACK. The read operation is thus started and completed within two processor cycles (160 ns). $\overline{HBE}$ is released during high byte read. This allows the processor to read the lower byte of data as soon as high byte read is complete. The low byte read operation executes in a similar manner to the first and is completed during the next 160 ns.

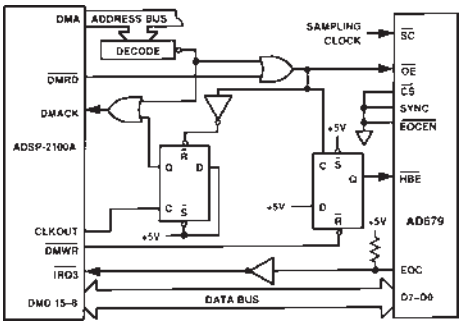
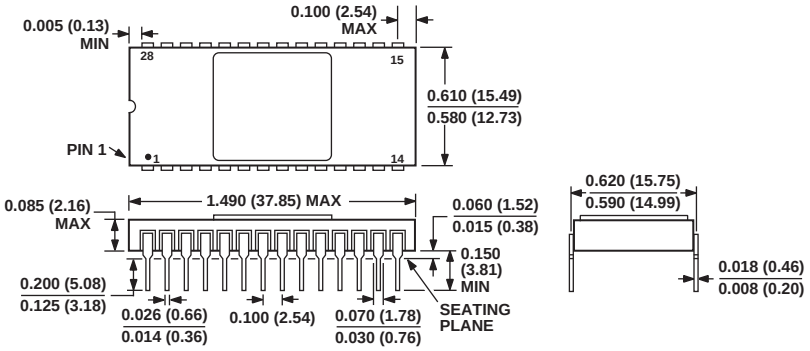



*Figure 12. AD679 to ADSP-2100A Interface*

## OUTLINE DIMENSIONS

### 28-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]
### (D-28)

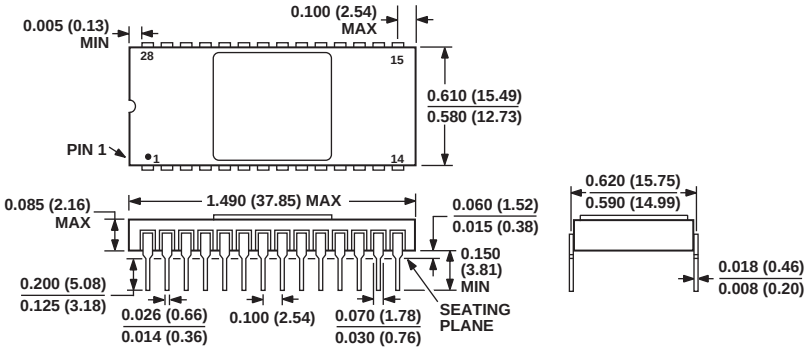
Dimensions shown in inches and (millimeters)




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

### 28-Lead Plastic Dual In-Line Package [PDIP]
### Wide Body
### (N-28)

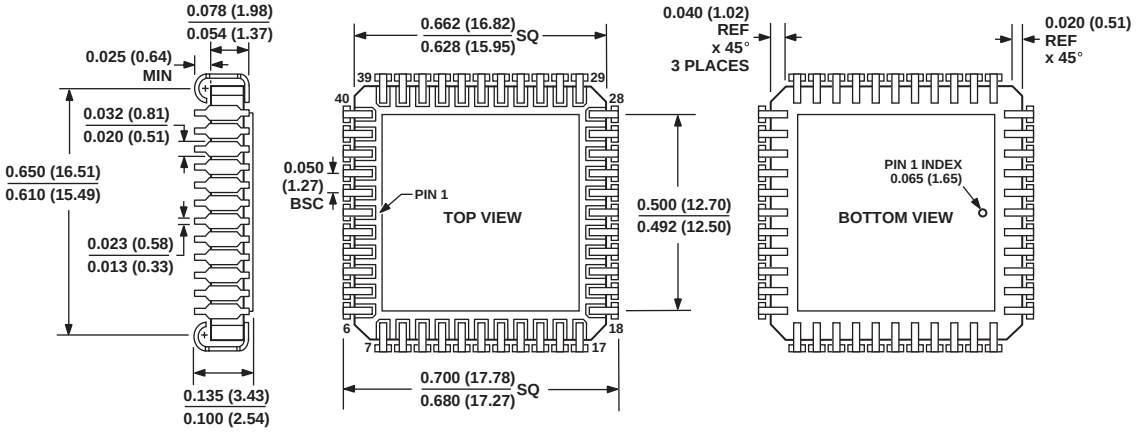
Dimensions shown in inches and (millimeters)




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

**OUTLINE DIMENSIONS**

**44-Lead Ceramic Leaded Chip Carrier, J-Formed Leads [JLCC]**
**(J-44)**
Dimensions shown in inches and (millimeters)




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

# Revision History

| Location | Page |
|---|---|
| **6/04—Data Sheet changed from REV. C to REV. D.** | |
| Updated Format | Universal |
| Changes to FEATURES | 1 |
| Changes to AC SPECIFICATIONS | 2 |
| Changes to DC SPECIFICATIONS | 3 |
| Changes to ORDERING GUIDE | 5 |
| Updated OUTLINE DIMENSIONS | 14 |

# Mouser Electronics

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AD679BJ AD679BD AD679JN AD679SJ/883B AD679JNZ AD679AJ AD679KD AD679JD AD679TD/883B AD679KNZ