REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

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TITLE
MICROCIRCUIT, LINEAR, 20 V, ULTRALOW NOISE, ULTRAHIGH PSRR LINEAR REGULATOR, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/21614

REV

PAGE 1 OF 16

AMSC N/A

5962-V037-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 20 V, ultralow noise, ultrahigh power supply rejection ratio (PSRR) linear regulator microcircuit, with an operating temperature range of -55°C to +150°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21614	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	LT3045-EP	20 V, ultralow noise, ultrahigh PSRR linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	12	See figure 1	Plastic micro small outline package (MSOP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

IN pin voltage	±22 V
EN/UV pin voltage	±22 V
IN to EN/UV differential voltage	±22 V
PG pin voltage	-0.3 V, 22 V 2/
ILIM pin voltage	-0.3 V, 1 V 2/
PGFB pin voltage	-0.3 V, 22 V 2/
SET pin voltage	-0.3 V, 16 V 2/
SET pin current	±20 mA 3/
OUTS pin voltage	-0.3 V, 16 V 2/
OUTS pin current	±20 mA 3/
OUT pin voltage	-0.3 V, 16 V 2/
OUT to OUTS differential	±1.2 V 4/
IN to OUT differential voltage	±22 V
IN to OUTS differential voltage	±22 V
Output short circuit duration	Indefinte
Junction temperature range (T_J)	-55°C to +150°C 5/
Junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	8°C/W
Thermal resistance, junction to ambient (θ_{JA})	33°C/W

1.4 Recommended operating conditions. 6/

Operating free-air temperature range (T_A)	-55°C to +150°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Parasitic diodes exist internally between the ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive these pins more than 0.3 V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

3/ SET and OUTS pins are clamped using diodes and two 25 Ω series resistors. For less than 5 ms transients, this clamp circuitry can carry more than the rated current. Refer to device Applications Information for more information.

4/ Maximum OUT to OUTS differential is guaranteed by design.

5/ The device is tested and specified under pulsed load conditions such that TJ ≈ TA. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input voltage range			-55°C to +150°C	01	2	20	V
Minimum IN pin 2/ voltage		I_{LOAD} = 500 mA, V_{IN} UVLO rising	-55°C to +150°C	01		2	V
					1.78 typical		
		V_{IN} UVLO hysteresis	+25°C		75 typical		mV
Output voltage reference		$V_{IN} > V_{OUT}$	-55°C to +150°C	01	0	15	V
SET pin current	I_{SET}	V_{IN} = 2 V, I_{LOAD} = 1 mA, V_{OUT} = 1.3 V	+25°C	01	99	101	µA
					100 typical		
		2 V < V_{IN} < 20 V, 0 V < V_{OUT} < 15 V, 1 mA < I_{LOAD} < 500 mA 3/	-55°C to +150°C		98	102	
					100 typical		
Fast start up set pin current		V_{PGFB} = 289 mV, V_{IN} = 2.8 V, V_{SET} = 1.3 V	+25°C	01	2 typical		mA
Output offset voltage (V_{OUT} – V_{SET}) 4/	V_{OS}	V_{IN} = 2 V, I_{LOAD} = 1 mA, V_{OUT} = 1.3 V	+25°C	01	-1	1	mV
		2 V < V_{IN} < 20 V, 0 V < V_{OUT} < 15 V, 1 mA < I_{LOAD} < 500 mA 3/	-55°C to +150°C		-2	2	
Line regulation	ΔISET	V_{IN} = 2 V to 20 V, I_{LOAD} = 1 mA, V_{OUT} = 1.3 V	-55°C to +150°C	01		±2	nA/V
					0.5 typical		
	ΔVOS	V_{IN} = 2 V to 20 V, I_{LOAD} = 1 mA, V_{OUT} = 1.3 V 4/				±3	µV/V
					0.5 typical		
Load regulation	ΔISET	I_{LOAD} = 1 mA to 500 mA, V_{IN} = 2 V, V_{OUT} = 1.3 V	+25°C	01	3 typical		nA
	ΔVOS	I_{LOAD} = 1 mA to 500 mA, V_{IN} = 2 V, V_{OUT} = 1.3 V 4/	-55°C to +150°C			0.5	mV
					0.1 typical		
Change in I_{SET} with V_{SET}		V_{SET} = 1.3 V to 15 V, V_{IN} = 20 V, I_{LOAD} = 1 mA	-55°C to +150°C	01		400	nA
					30 typical		
Change in V_{OS} with V_{SET}		V_{SET} = 1.3 V to 15 V, V_{IN} = 20 V, I_{LOAD} = 1 mA 4/	-55°C to +150°C	01		0.6	mV
					0.03 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Change in I_{SET} with V_{SET}		V_{SET} = 0 V to 1.3 V, V_{IN} = 20 V, I_{LOAD} = 1 mA	-55°C to +150°C	01		600	nA
					150 typical		
Change in V_{OS} with V_{SET}		V_{SET} = 0 V to 1.3 V, V_{IN} = 20 V, I_{LOAD} = 1 mA 4/	-55°C to +150°C	01		2	mV
					0.3 typical		
Dropout voltage		I_{LOAD} = 1 mA, 50 mA	+25°C	01		275	mV
					220 typical		
			-55°C to +150°C			330	
		I_{LOAD} = 300 mA 5/	+25°C			280	
					220 typical		
			-55°C to +150°C			350	
		I_{LOAD} = 500 mA 5/	+25°C			350	
					260 typical		
			-55°C to +150°C			450	
GND pin current 6/ V_{IN} = $V_{OUT(NOM)}$		I_{LOAD} = 10 μA	25°C	01	2.2 typical		mA
		I_{LOAD} = 1 mA	-55°C to +150°C			4	
					2.4 typical		
		I_{LOAD} = 50 mA	-55°C to +150°C			5.5	
					3.5 typical		
		I_{LOAD} = 100 mA	-55°C to +150°C			7	
					4.3 typical		
		I_{LOAD} = 500 mA	-55°C to +150°C			25	
					15 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output noise 4/ 7/ spectral density		I_{LOAD} = 500 mA, frequency = 10 Hz, C_{OUT} = 10 µF, C_{SET} = 0.47 µF, V_{OUT} = 3.3 V	25°C	01	500 typical		$nV/\sqrt{Hz}$
		I_{LOAD} = 500 mA, frequency = 10 Hz, C_{OUT} = 10 µF, C_{SET} = 4.7 µF, 1.3 V ≤ V_{OUT} ≤ 15 V			70 typical		
		I_{LOAD} = 500 mA, frequency = 10 kHz, C_{OUT} = 10 µF, C_{SET} = 0.47 µF, 1.3 V ≤ V_{OUT} ≤ 15 V			2 typical		
		I_{LOAD} = 500 mA, frequency = 10 kHz, C_{OUT} = 10 µF, C_{SET} = 0.47 µF, 0 V ≤ V_{OUT} < 1.3 V			5 typical		
Output RMS 4/ 7/ noise		I_{LOAD} = 500 mA, BW = 10 Hz to 100 kHz, C_{OUT} = 10 µF, C_{SET} = 0.47 µF, V_{OUT} = 3.3 V	25°C	01	2.5 typical		μV_{RMS}
		I_{LOAD} = 500 mA, BW = 10 Hz to 100 kHz, C_{OUT} = 10 µF, C_{SET} = 4.7 µF, 1.3 V ≤ V_{OUT} ≤ 15 V			0.8 typical		
		I_{LOAD} = 500 mA, BW = 10 Hz to 100 kHz, C_{OUT} = 10 µF, C_{SET} = 4.7 µF, 0 V ≤ V_{OUT} < 1.3 V			1.8 typical		
Reference 4/ 7/ current RMS output noise		BW = 10 Hz to 100 kHz	25°C	01	6 typical		nA_{RMS}

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Ripple rejection 4/ 7/ 1.3 V ≤ V_{OUT} ≤ 15 V, $V_{IN} - V_{OUT}$ = 2 V Avg		V_{RIPPLE} = 500 mV_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 4.7 µF	25°C	01	117 typical		dB
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 10 kHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			90 typical		
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 100 kHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			77 typical		
		V_{RIPPLE} = 150 mV_{P-P}, f_{RIPPLE} = 1 MHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			76 typical		
		V_{RIPPLE} = 80 mV_{P-P}, f_{RIPPLE} = 10 MHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			53 typical		
Ripple rejection 4/ 7/ 0 V ≤ V_{OUT} ≤ 1.3 V, $V_{IN} - V_{OUT}$ = 2 V Avg		V_{RIPPLE} = 500 mV_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF	25°C	01	104 typical		dB
		V_{RIPPLE} = 50 mV_{P-P}, f_{RIPPLE} = 10 kHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			85 typical		
		V_{RIPPLE} = 50 mV_{P-P}, f_{RIPPLE} = 100 kHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			72 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Ripple rejection 4/ 7/ 1.3 V ≤ V_{OUT} ≤ 15 V, V_{IN} – V_{OUT} = 2 V Avg		V_{RIPPLE} = 50 mV_{P-P}, f_{RIPPLE} = 1 MHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF	25°C	01	64 typical		dB
		V_{RIPPLE} = 50 mV_{P-P}, f_{RIPPLE} = 10 MHz, I_{LOAD} = 500 mA, C_{OUT} = 10 µF, C_{SET} = 0.47 µF			54 typical		
EN/UV pin threshold		EN/UV trip point rising (turn on)	-55°C to +150°C	01	1.18	1.32	V
		V_{IN} = 2 V			1.24 typical		
EN/UV pin hysteresis		EN/UV trip point hysteresis, V_{IN} = 2 V	25°C	01	130 typical		mV
EN/UV pin current		$V_{EN/UV}$ = 0 V, V_{IN} = 20 V	-55°C to +150°C	01		±1	µA
		$V_{EN/UV}$ = 1.24 V, V_{IN} = 20 V	25°C		0.03 typical		
		$V_{EN/UV}$ = 20 V, V_{IN} = 0 V	-55°C to +150°C			15	
					8 typical		
Quiescent current in shutdown ($V_{EN/UV}$ = 0 V)		V_{IN} = 6 V	25°C	01		1	µA
					0.3 typical		
			$T_J \leq$ +150°C			20	
Internal current limit 8/		V_{IN} = 2 V, V_{OUT} = 0 V	-55°C to +150°C	01	570	850	mA
					710 typical		
		V_{IN} = 12 V, V_{OUT} = 0 V	25°C		700 typical		
		VIN = 20 V, VOUT = 0 V	-55°C to +150°C		230	430	
					330 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Programmable current limit		Programming Scale Factor: 2 V < V_{IN} < 20 V 9/	25°C	01	150 typical		mA•kΩ
		V_{IN} = 2 V, V_{OUT} = 0 V, R_{ILIM} = 300 Ω	-55°C to +150°C		450	550	mA
					500 typical		
		V_{IN} = 2 V, V_{OUT} = 0 V, R_{ILIM} = 1.5 kΩ			90	110	
					100 typical		
Power good feedback (PGFB) trip point		PGFB trip point rising	-55°C to +150°C	01	291	309	mV
					300 typical		
PGFB hysteresis		PGFB trip point hysteresis	25°C	01	7 typical		mV
PGFB pin current		V_{IN} = 2 V, V_{PGFB} = 300 mV (current flows out of pin)	25°C	01	25 typical		nA
Power good (PG) output low voltage		I_{PG} = 100 µA	-55°C to +150°C	01		100	mV
					30 typical		
PG leakage current		V_{PG} = 20 V	-55°C to +150°C	01		1	µA
Reverse input current		V_{IN} = –20 V, $V_{EN/UV}$ = 0 V, V_{OUT} = 0 V, V_{SET} = 0 V	-55°C to +150°C	01		100	µA
Reverse output current		V_{IN} = 0 V, V_{OUT} = 5 V, SET = Open	25°C	01		25	µA
					14 typical		
Minimum load 10/ required		V_{OUT} < 1 V	-55°C to +150°C	01	10		µA
Thermal shutdown		T_J rising		01	165 typical		°C
		Hysteresis			8 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Start up time		$V_{OUT(NOM)}$ = 5 V, I_{LOAD} = 500 mA, C_{SET} = 0.47 µF, V_{IN} = 6 V, V_{PGFB} = 6 V	25°C	01	55 typical		ms
		$V_{OUT(NOM)}$ = 5 V, I_{LOAD} = 500 mA, C_{SET} = 4.7 µF, V_{IN} = 6 V, V_{PGFB} = 6 V			550 typical		
		$V_{OUT(NOM)}$ = 5 V, I_{LOAD} = 500 mA, C_{SET} = 4.7 µF, V_{IN} = 6 V, RPG1 = 50 kΩ, RPG2 = 700 kΩ (with fast start-up to 90% of V_{OUT})			10 typical		
Thermal regulation		10 ms pulse	25°C	01	-0.01 typical		%/W

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The EN/UV pin threshold must be met to ensure device operation.

3/ Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current limit foldback which starts to decrease current limit at $V_{IN} – V_{OUT}$ > 12 V. If operating at maximum output current, limit the input voltage range. If operating at the maximum input voltage, limit the output current range.

4/ OUTS ties directly to OUT.

5/ Dropout voltage is the minimum input to output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when $V_{IN} = V_{OUT(NOMINAL)}$. For lower output voltages, below 1.5 V, dropout voltage is limited by the minimum input voltage specification. Please consult the device typical performance characteristics for curves of dropout voltage as a function of output load current and temperature measured in a typical application circuit.

6/ GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst case GND pin current. GND pin current decreases at higher input voltages. Note that GND pin current does not include SET pin or ILIM pin current but, quiescent current does include them.

7/ Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The output noise then equals the error amplifier noise. Use of a SET pin bypass capacitor also increases start-up time.

TABLE I. Electrical performance characteristics – Continued. 1/

8/ The internal back up current limit circuitry incorporates fold back protection that decreases current limit for $V_{IN} – V_{OUT} > 12$ V. Some level of output current is provided at all $V_{IN} – V_{OUT}$ differential voltages. Consult the device typical performance characteristics graph for current limit versus $V_{IN} – V_{OUT}$.

9/ The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{IN} – V_{OUT}$ differentials greater than 12 V.

10/ For output voltages less than 1 V, the device requires a 10 µA minimum load current for stability.

Case X

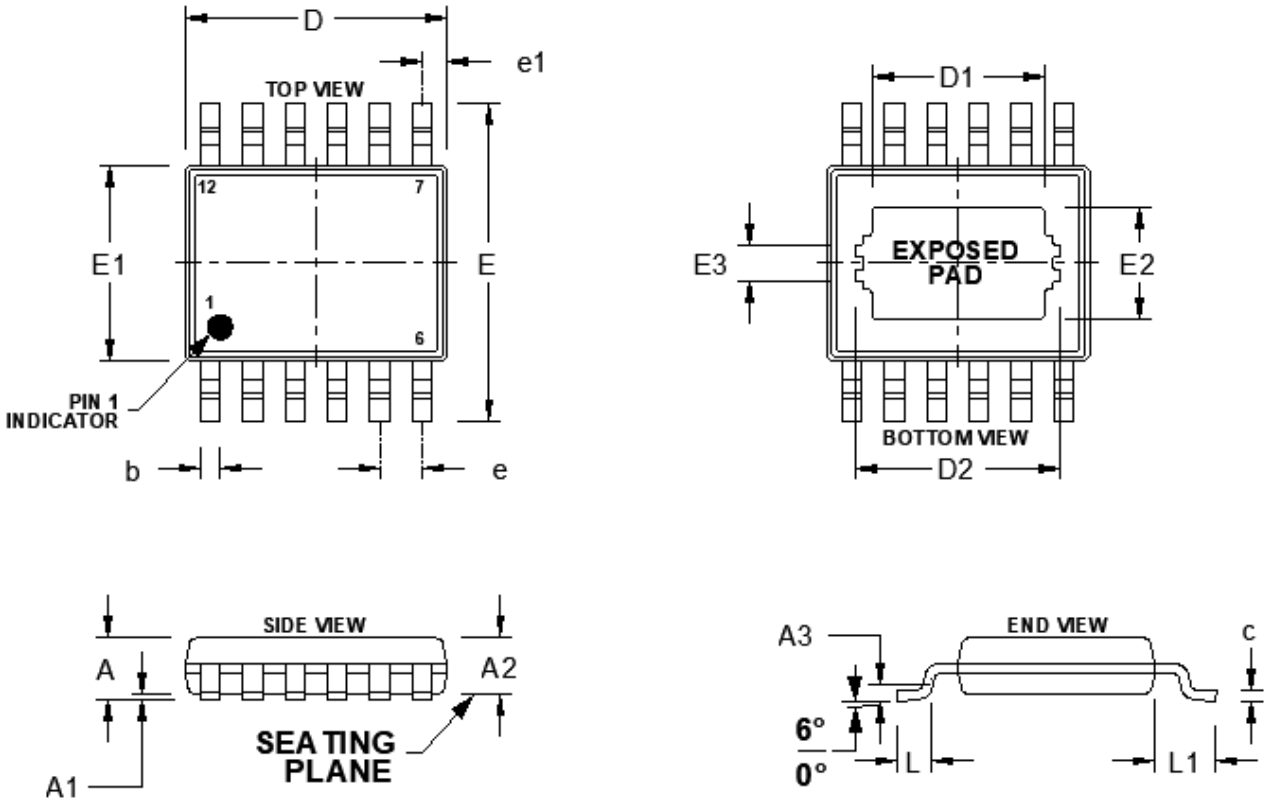

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CAGE CODE 16236	DWG NO. V62/21614
		REV	PAGE 13

Symbol	Dimensions			
	Inches		Millimeter	
	Minimum	Maximum	Minimum	Maximum
A	---	.043	---	1.10
A1	.002	.006	0.05	0.15
A2	.034 REF		0.86 REF	
A3	.010 GAGE PLANE		0.25 GAGE PLANE	
c	.005	.009	0.127	0.230
D	.155	.163	3.937	4.141
D1	.104 REF		2.65 REF	
D2	.124 REF		3.15 REF	
e	.025 REF		0.65 REF	
e1	.015 REF		0.395 REF	
E	.187	.199	4.748	5.052
E1	.114	.122	2.898	3.102
E2	.067 REF		1.70 REF	
E3	.032 REF		0.81 REF	
L	.015	.027	0.378	0.682
L1	.037 REF		0.95 REF	

NOTE:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	IN	Input. This pin supplies power to the regulator.
2	IN	Input. This pin supplies power to the regulator.
3	IN	Input. This pin supplies power to the regulator.
4	EN/UV	Enable/UVLO. Pulling the device's EN/ UV pin low places the part in shutdown. Quiescent current in shutdown drops to less than 1 µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV and GND. The device typically turns on when the EN/UV voltage exceeds 1.24 V on its rising edge, with a 130 mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, tie EN/UV to IN. Do not float the EN/UV pin
5	PG	Power good. PG is an open collector flag that indicates output voltage regulation.
6	ILIM	Current limit programming pin. Connecting a resistor between ILIM and GND programs the current limit.
7	PGFB	Power good feedback. The PG pin pulls high if PGFB increases beyond 300 mV on its rising edge, with 7 mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB and GND sets the programmable power good threshold with the following transfer function: 0.3 V • (1 + RPG2/RPG1). In the device applications information section, PGFB also activates the fast start up circuitry. Tie PGFB to IN if power good and fast start-up functionalities are not needed, and if reverse input protection is additionally required, tie the anode of a 1N4148 diode to IN and its cathode to PGFB. See the device typical applications section for details. A parasitic substrate diode exists between PGFB and GND pins of the device; do not drive PGFB more than 0.3 V below GND during normal operation or during a fault condition.
8	SET	SET. This pin is the inverting input of the error amplifier and regulation set point for the device.
9	GND	Ground.
10	OUTS	Output sense. This pin is the noninverting input to the error amplifier.
11	OUT	Output. This pin supplies power to the load.
12	OUT	Output. This pin supplies power to the load.
13	EXPOSED PAD	Ground. The exposed backside is an electrical connection to GND.

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21614-01XE	24355	Tube, 37 units	3045EP	LT3045HMSE#Z-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LT3045EMSE#PBF LT3045EDD#TRPBF LT3045IDD#PBF LT3045HDD#PBF