Multiphase Boost Converter Expander with Internal Gate Drivers

FEATURES

- **Expands Up to 4 Phases per Chip**
- **Up to 80V Input or Output Voltage**
- **Cascade with Multiple Chips for High Current Applications**
- **Supports Up to 18 Distinct Phases from 20° to 180°**
- **Phases Can Share Phase Angle**
- **Excellent DC and Transient Current Sharing**
- Phase-Lockable Fixed Frequency 125kHz to 1MHz
- Supports Bidirectional Current Flow
- R_{SENSE} or DCR Current Sensing
- Eliminates the Need to Route Sensitive Feedback and Control Signals.
- 52-Lead (7mm × 8mm) QFN Package

APPLICATIONS

- High Current Distributed Power Systems
- Telecom, Datacom, and Storage Systems
- Industrial and Automotive

DESCRIPTION

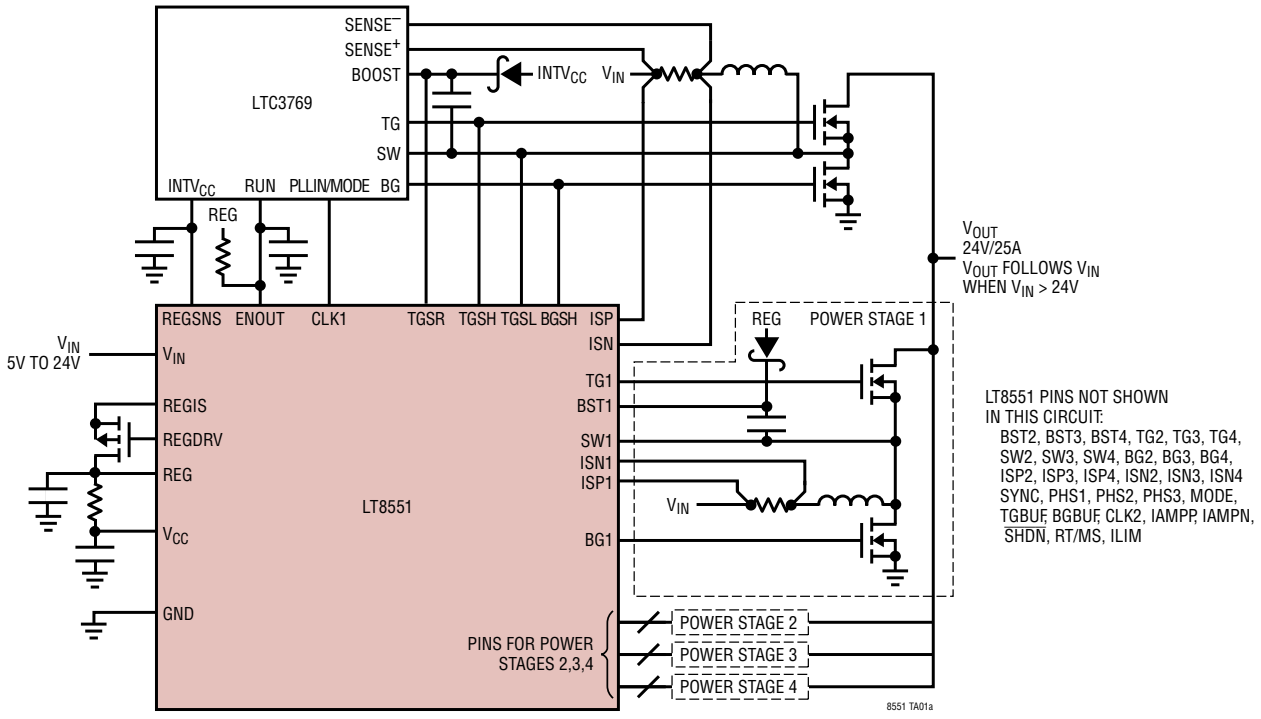
The LT®8551 is a multiphase expander for synchronous boost DC/DC converters. It operates in tandem with any synchronous boost DC/DC converter to increase the load current capability by adding additional phases, which are clocked out-of-phase to reduce ripple current and filtering capacitance. It easily adds phases without the need to route sensitive feedback and control signals.

The LT8551 integrates 5V gate drivers and can support up to four boost phases per device. Multiple LT8551 devices can be used for up to 18 phases. It accurately monitors and adjusts the current of each channel to achieve excellent DC and transient current sharing.

The LT8551 operates over a fixed frequency from 100kHz to 1MHz or can be synchronized to an external clock.

TYPICAL APPLICATION

24V/25A Step-Up Expander System



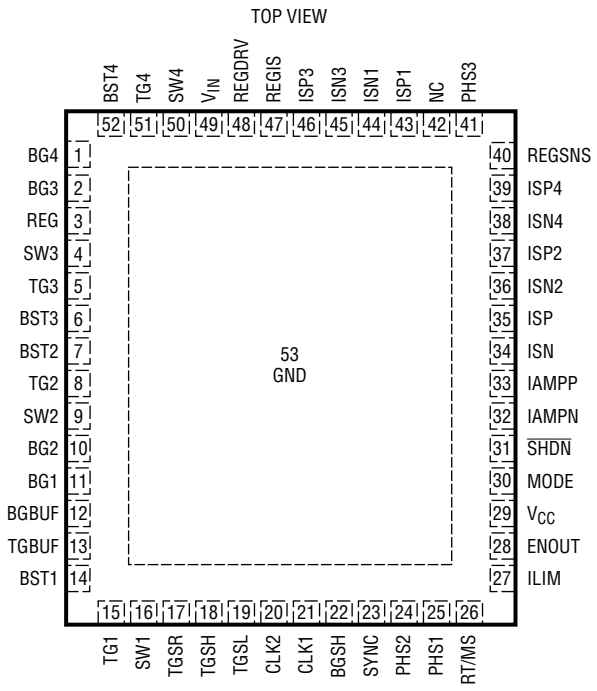
Rev 0

ABSOLUTE MAXIMUM RATINGS

(Note 1)

SW1/2/3/4 (Note 5)……..80V
ISP1/2/3/4, ISN1/2/3/4, ISP, ISN, V_{IN},
REGIS, REGDRV Voltage (Note 2)..... .–0.3V to 80V
$\overline{SHDN}$ Voltage……–0.3V to 70V
TGSL Voltage……–3V to 80V
TGSH Voltage……–3V to 86V
TG1/2/3/4, BST1/2/3/4, TGSR Voltage ..... . –0.3V to 86V
BG1/2/3/4, RT/MS, SYNC, PHS1/2/3, CLK1/2,
REGSNS, IAMPP, ILIM, BGSH, BGBUF, TGBUF,
ENOUT, MODE, V_{CC}, REG, (BST–SW)1/2/3/4,
(TG–SW)1/2/3/4, (V_{IN}–REGDRV),
(TGSR–TGSL), (TGSH–TGSL) Voltage .. –0.3V to 6.0V
IAMPN Voltage…… –0.6V to 0.6V
(ISP–ISN)1/2/3/4, (ISP–ISN) Voltage …... –0.3V to 0.3V
Operating Junction Temperature Range (Note 3)
LT8551E..... –40°C to 125°C
LT8551I..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 31°C/W, θ_{JC} = 2°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8551EUKG#PBF	LT8551EUKG#TRPBF	8551	52-Pin (7mm × 8mm) Plastic QFN	–40°C to 125°C
LT8551IUKG#PBF	LT8551IUKG#TRPBF	8551	52-Pin (7mm × 8mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, REG = 5V, V_{CC} = 5V, $\overline{SHDN}$ = High, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range	For Min Spec, V_{CC}, REG = 0V	●	3.6		80	V
V_{IN} Quiescent Current	REG = V_{CC} = 5V, REGDRV, REGIS Floating			800		µA
V_{IN} Quiescent Current in Shutdown					2	µA
V_{CC} Quiescent Current	Not Switching			5		mA
V_{CC} Undervoltage Lockout	V_{CC} Falling, REG = V_{CC}	●	3.3	3.55	3.8	V
V_{CC} Undervoltage Lockout Hysteresis	REG = V_{CC}			0.1		V
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Falling	●	1.05	1.15	1.25	V
$\overline{SHDN}$ Input Voltage High Hysteresis				60		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current, V_{CC} = REG = 3V	●			0.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 8.5	1 20	µA µA
MODE Low Falling Threshold	Slave LT8551	●	0.5			V
MODE High Rising Threshold	Slave LT8551	●			4.5	V
MODE Output Voltage Low	Master LT8551, 200µA into MODE pin			50		mV
MODE Output Voltage High	Master LT8551, 20µA out of MODE pin			4.8		V
MODE Pin Impedance in Middle State	Master LT8551			9		kΩ
ENOUT Output Voltage Low	Master LT8551, 1mA into ENOUT Pin, V_{CC}, REG in UVLO			60		mV
ENOUT Leakage Current	ENOUT = 5V, REG = V_{CC} = 3V			0.2	1	µA
ENOUT Rising Threshold				2.1		V
ENOUT Threshold Hysteresis				0.4		V
Current Sensing						
Maximum Positive Current Sense Voltage, (ISP*n*–ISN*n*)	ILIM = 0V, ISN*n* = 12V, ISP*n* Rising ILIM = REG, ISN*n* = 12V, ISP*n* Rising ILIM = Float, ISN*n* = 12V, ISP*n* Rising	● ● ●	27.0 56 84.5	30 60 90	32.5 64 95.5	mV mV mV
Maximum Negative Current Sense Voltage, (ISN*n*–ISP*n*)	ILIM = 0V, ISN*n* = 12V, ISP*n* Falling ILIM = REG, ISN*n* = 12V, ISP*n* Falling ILIM = Float, ISN*n* = 12V, ISP*n* Falling	● ● ●	26.5 55.5 84	30 60 90	33 64.5 96	mV mV mV
ISP, ISN Common Mode Operating Voltage Range		●	0		80	V
ISP*n*, ISN*n* Common Mode Operating Voltage Range		●	0		80	V
ILIM High Rising Threshold		●			4.65	V
ILIM High Threshold Hysteresis				90		mV
ILIM Low Falling Threshold		●	0.3			V
ILIM Low Threshold Hysteresis				80		mV
ILIM Impedance at Floating				11		kΩ
IAMPP Output Voltage	(ISP–ISN) = 30mV, ILIM = 0V, Master LT8551, ISP = 12V (ISP–ISN) = 0mV, ILIM = 0V, Master LT8551, ISP = 12V (ISP–ISN) = –30mV, ILIM = 0V, Master LT8551, ISP = 12V (ISP–ISN) = 60mV, ILIM = REG, Master LT8551, ISP = 12V (ISP–ISN) = 0mV, ILIM = REG, Master LT8551, ISP = 12V (ISP–ISN) = –60mV, ILIM = REG, Master LT8551, ISP = 12V (ISP–ISN) = 90mV, ILIM = Float, Master LT8551, ISP = 12V (ISP–ISN) = 0mV, ILIM = Float, Master LT8551, ISP = 12V (ISP–ISN) = –90mV, ILIM = Float, Master LT8551, ISP = 12V	● ● ● ● ● ● ● ● ●	2.33 1.33 0.33 2.33 1.35 0.34 2.33 1.35 0.34	2.4 1.4 0.4 2.4 1.4 0.4 2.4 1.4 0.4	2.47 1.47 0.47 2.47 1.45 0.46 2.47 1.45 0.46	V V V V V V V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, REG = 5V, V_{CC} = 5V, $\overline{SHDN}$ = High, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
(ISP*n*–ISN*n*) Voltage In Regulation	IAMPP = 2.20V, IAMPN = 0V, ILIM = 0V, ISN*n* = 12V	●	21.25		26.75	mV
	IAMPP = 0.60V, IAMPN = 0V, ILIM = 0V, ISN*n* = 12V	●	–26.75		–21.25	mV
	IAMPP = 2.20V, IAMPN = 0V, ILIM = REG, ISN*n* = 12V	●	45		51	mV
	IAMPP = 0.60V, IAMPN = 0V, ILIM = REG, ISN*n* = 12V	●	–51		–45	mV
	IAMPP = 2.20V, IAMPN = 0V, ILIM = Float, ISN*n* = 12V	●	67.25		76.75	mV
	IAMPP = 0.60V, IAMPN = 0V, ILIM = Float, ISN*n* = 12V	●	–76.75		–67.25	mV
(ISP–ISN) to IAMPP Voltage Gain	ILIM = 0V, Master LT8551, ISP = 0V			33.3		
	ILIM = REG, Master LT8551, ISP = 0V			16.7		
	ILIM = FLOAT, Master LT8551, ISP = 0V			11.1		
IAMPP Sourcing Current Limit	(ISP–ISN) = 0mV, Master LT8551	●	250			µA
IAMPP Sinking Current Limit	(ISP–ISN) = 0mV, Master LT8551	●	60			µA
IAMPP Load Regulation	ILOAD = –200µA to 50 µA, Master LT8551				1	mV
IAMPP Pin Bias Current	IAMPP = 1.2V, Slave LT8551			3		µA
	IAMPP = 2.4V, Slave LT8551			6		µA
Mismatch Between (ISP*n*–ISN*n*) and Master LT8551's (ISP–ISN) in Regulation	ILIM = REG	●	–6		6	%
		●	–4.75		4.75	%
Mismatch Between (ISP*n*–ISN*n*) and Master LT8551's (ISP–ISN) in Regulation	ILIM = FLOAT	●	–6		6	%
		●	–5.5		5.5	%
Mismatch Between (ISP*n*–ISN*n*) and Master LT8551's (ISP–ISN) in Regulation	ILIM = 0V	●	–10		10	%
		●	–8		8	%
Oscillator						
CLK1 Frequency	RT/MS = 24.3kΩ, Master LT8551	●	900	1000	1100	kHz
	RT/MS = 100 kΩ, Master LT8551	●	236	250	264	kHz
	RT/MS = 249kΩ, Master LT8551	●	90	100	110	kHz
Switching Frequency Range	Free-Running	●	100		1000	kHz
	Synchronizing	●	125		1000	kHz
SYNC High Level for Synchronization		●	1.2			V
SYNC Low Level for Synchronization		●			0.8	V
CLK1, CLK2 Rise Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			7		ns
CLK1, CLK2 Fall Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			5		ns
CLK2 Rising Threshold	Slave LT8551	●			4	V
CLK2 Falling Threshold	Slave LT8551	●	1			V
PHS1, PHS2 High Rising Threshold		●			4.65	V
PHS1, PHS2 High Threshold Hysteresis				80		mV
PHS1, PHS2 Low Falling Threshold		●	0.3			V
PHS1, PHS2 Low Threshold Hysteresis				80		mV
PHS1, PHS2 Impedance at Floating				11		kΩ
PHS3 Rising Threshold		●			4.65	V
PHS3 Threshold Hysteresis				80		mV
REG LDO						
REG Voltage	REGSNS = 5V, IAMPN = 0V, I_{LOAD} = 45mA	●	4.9	5.1	5.3	V
REG LDO Current Limit	V_{IN} = 12V, REGSNS = 5V, REG, V_{CC} = 4V			250		mA
	V_{IN} = 24V, REGSNS = 5V, REG, V_{CC} = 4V			145		mA
REG LDO Gate Drive Clamp Voltage	(V_{IN} – REGDRV) Voltage, REG, V_{CC} = 4.5V			5.3		V
REG Load Regulation	I_{LOAD} = 0A to 100mA, REGSNS = 5V, IAMPN = 0V			90		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, REG = 5V, V_{CC} = 5V, $\overline{SHDN}$ = High, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REGSNS Pin Bias Current	REGSNS = 5V			12		µA
Gate Drivers						
TG1, TG2, TG3, TG4 Rise Time	C_{LOAD} = 3.3nF, SWx = 0V, BSTx = 5V (Note 4)			30		ns
TG1, TG2, TG3, TG4 Fall Time	C_{LOAD} = 3.3nF, SWx = 0V, BSTx = 5V (Note 4)			20		ns
BG1, BG2, BG3, BG4 Rise Time	C_{LOAD} = 3.3nF (Note 4)			50		ns
BG1, BG2, BG3, BG4 Fall Time	C_{LOAD} = 3.3nF (Note 4)			27		ns
Bottom & Top Gate Non-Overlap Time	TG Falling to BG Rising, C_{LOAD} = 3.3nF (Note 4) BG Falling to TG Rising, C_{LOAD} = 3.3nF (Note 4)			85 80		ns ns
Bottom & Top Gate Minimum Off-Time	C_{LOAD} = 3.3nF (Note 4)			140		ns
Primary Gate Sensing						
BGSH Rising Threshold		●			4	V
BGSH Falling Threshold		●	1			V
BGSH Threshold Hysteresis				1.4		V
BGSH to BGBUF Delay	C_{LOAD} = 220pF, Master LT8551 (Note 4)			45		ns
BGBUF Rise Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			8		ns
BGBUF Fall Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			6		ns
TGSH Rising Threshold	TGSR = 5V, TGSL = 0V	●			4	V
TGSH Falling Threshold	TGSR = 5V, TGSL = 0V	●	1			V
TGSH Threshold Hysteresis				1.4		V
TGSH to TGBUF Delay	C_{LOAD} = 220pF, Master LT8551 (Note 4)			45		ns
TGBUF Rise Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			8		ns
TGBUF Fall Time	C_{LOAD} = 220pF, Master LT8551 (Note 4)			6		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating Condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to REGDRV, BG1, BG2, BG3, BG4, TG1, TG2, TG3 and TG4, otherwise permanent damage may occur.

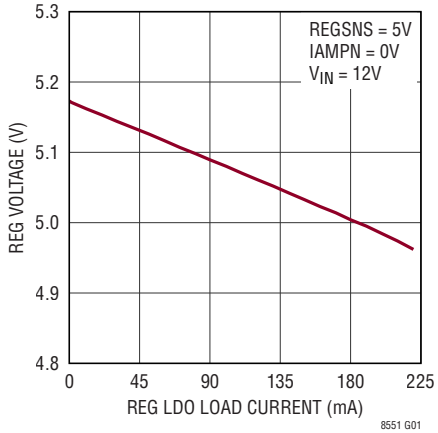
Note 3: The LT8551E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8551I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

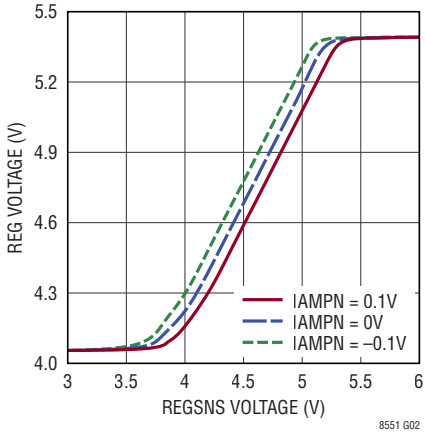
Note 5: Negative voltages on SW1/2/3/4 pins are limited, in an application, by the body diodes of the external NMOS devices, or the parallel Schottky diodes when present. The SW1/2/3/4 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

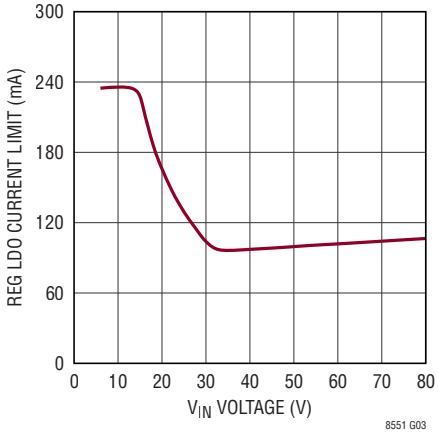
REG LDO Load Regulation



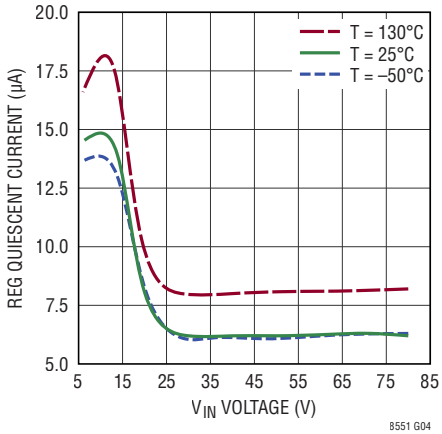
REG Voltage vs REGSNS Voltage



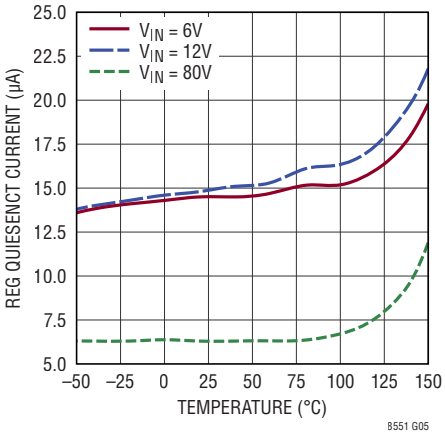
REG LDO Current Limit



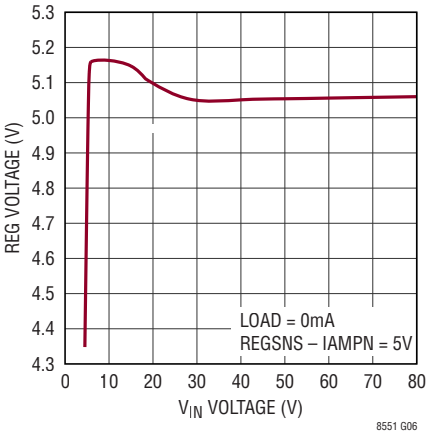
REG Quiescent Current vs V_{IN} Voltage, Not Switching



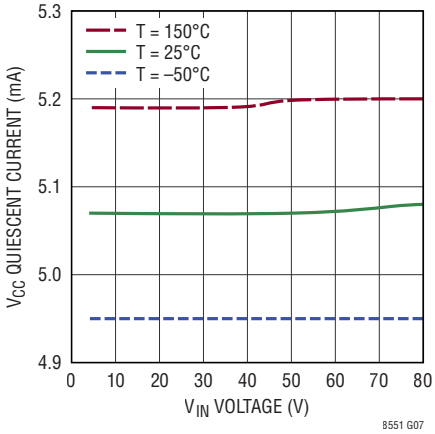
REG Quiescent Current vs Temperature, Not Switching



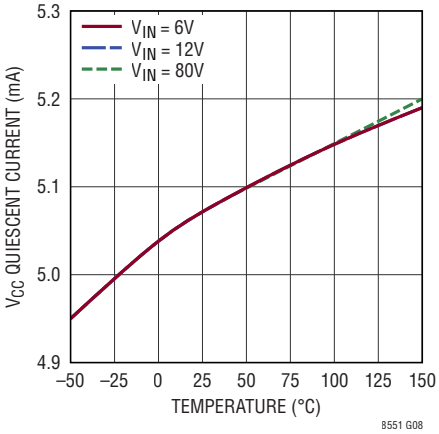
REG LDO Line Regulation



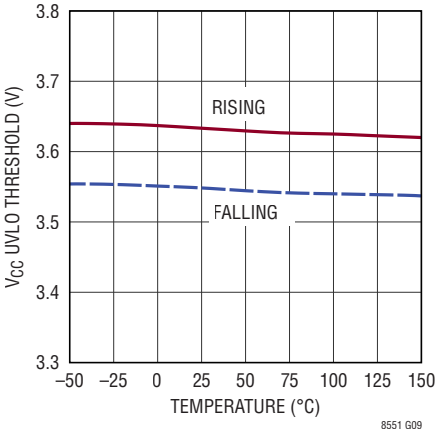
V_{CC} Quiescent Current vs V_{IN} Voltage, Not Switching



V_{CC} Quiescent Current vs Temperature, Not Switching

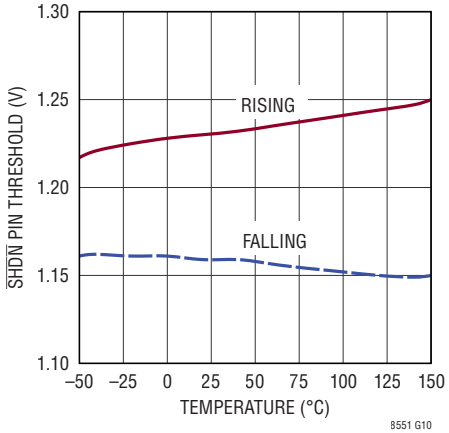


V_{CC} UVLO Threshold

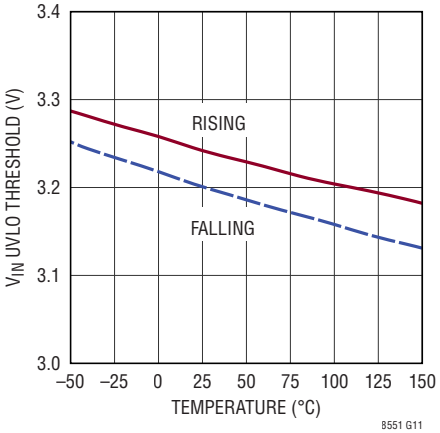


TYPICAL PERFORMANCE CHARACTERISTICS

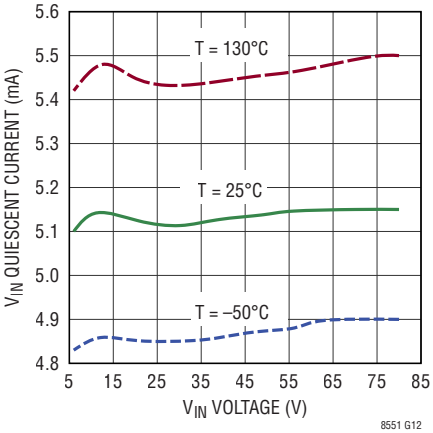
$\overline{SHDN}$ Pin Threshold



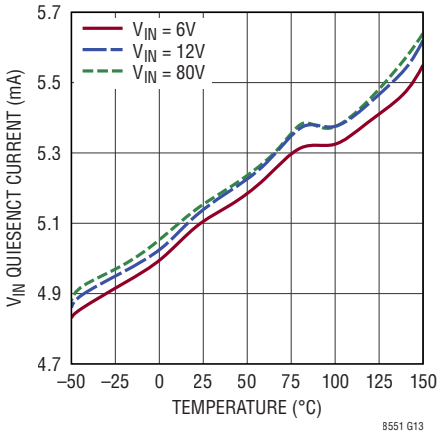
V_{IN} UVLO Threshold



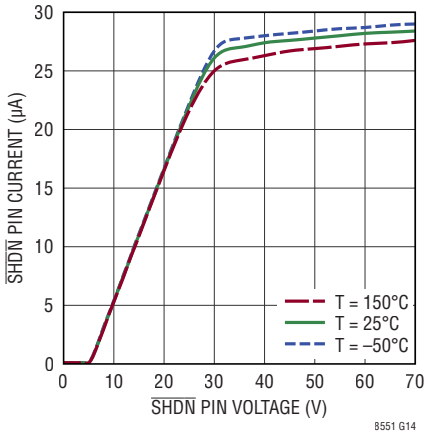
V_{IN} Quiescent Current vs V_{IN} Voltage, Not Switching



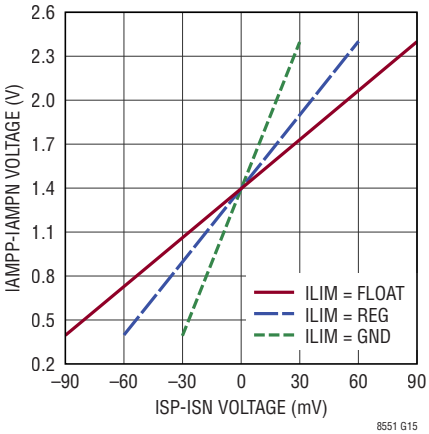
V_{IN} Quiescent Current vs Temperature, Not Switching



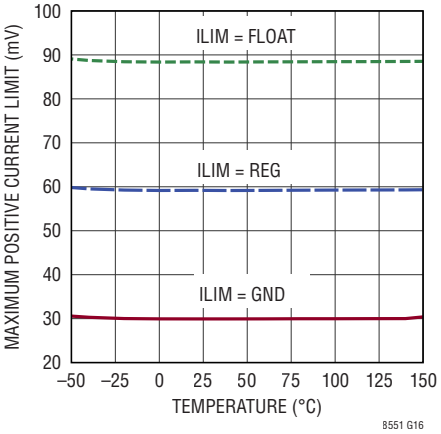
$\overline{SHDN}$ Pin Current vs Voltage



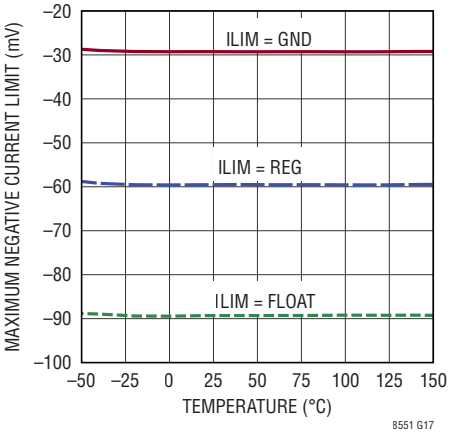
IAMPP–IAMPN Voltage vs (ISP–ISN) Voltage



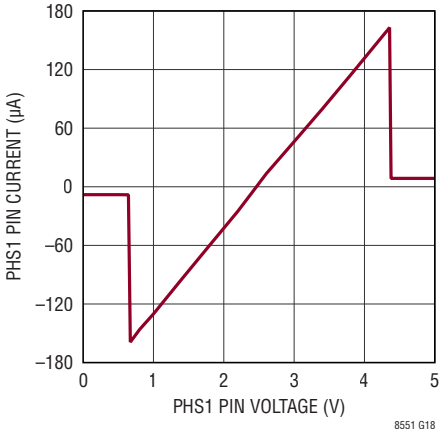
Maximum Positive Current Limit vs Temperature



Maximum Negative Current Limit vs Temperature

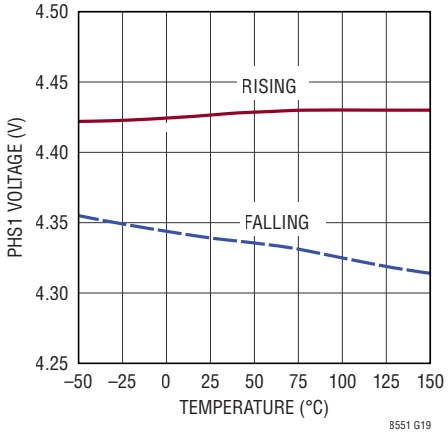


PHS1 Pin Current

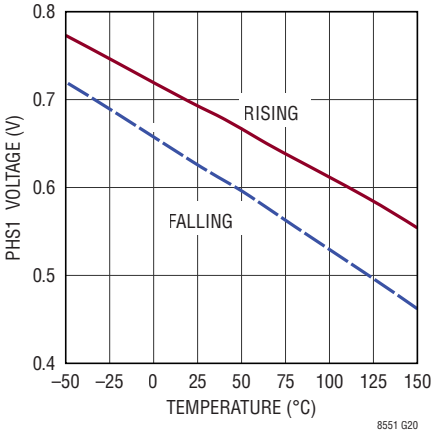


TYPICAL PERFORMANCE CHARACTERISTICS

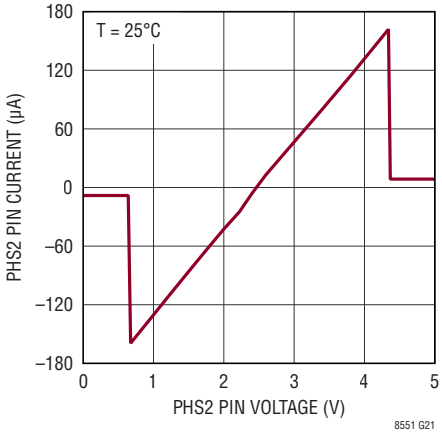
PHS1 High Threshold Voltage vs Temperature



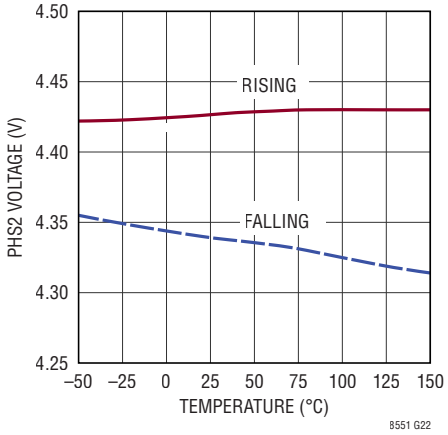
PHS1 Low Threshold Voltage vs Temperature



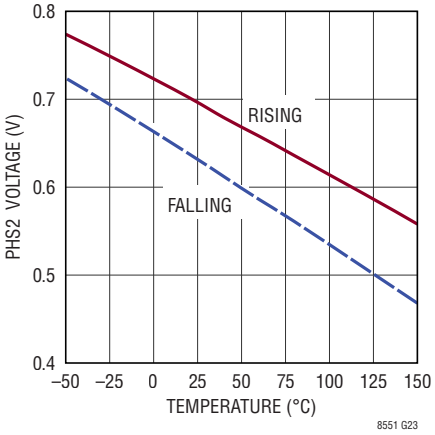
PHS2 Pin Current



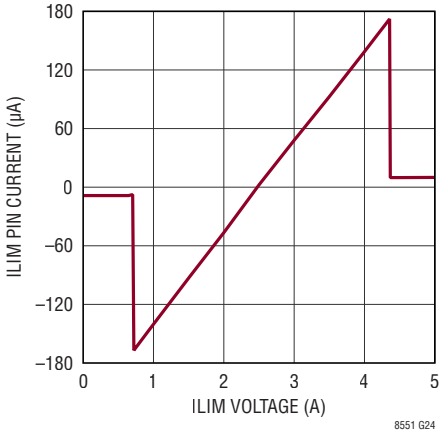
PHS2 High Threshold Voltage vs Temperature



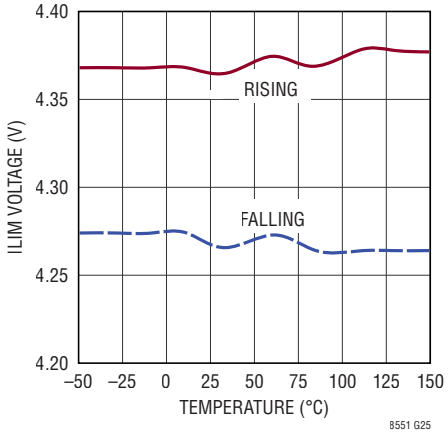
PHS2 Low Threshold Voltage vs Temperature



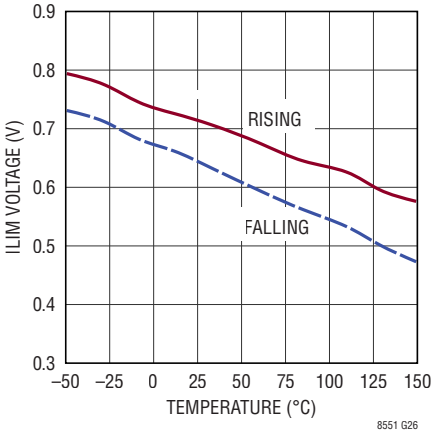
ILIM Pin Current vs Voltage



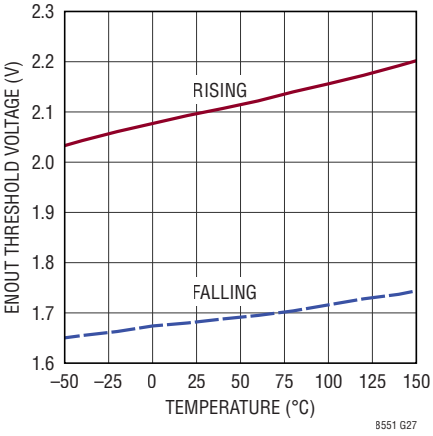
ILIM High Threshold Voltage vs Temperature



ILIM Low Threshold Voltage vs Temperature

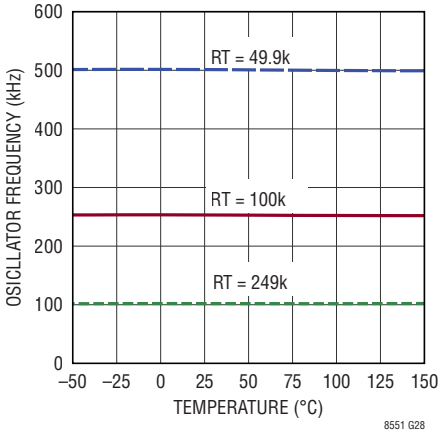


ENOUT Threshold Voltage

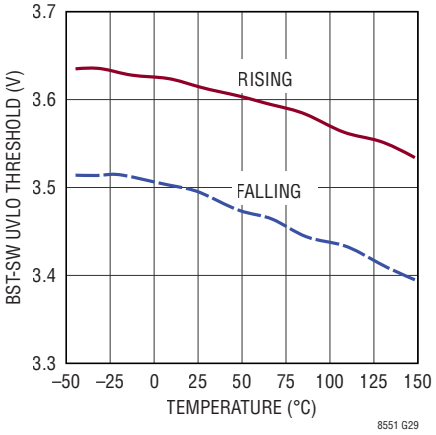


TYPICAL PERFORMANCE CHARACTERISTICS

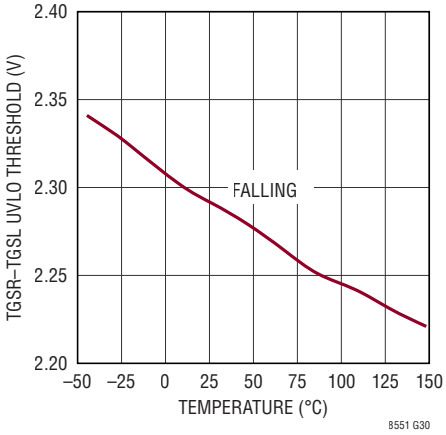
Oscillator Frequency vs Temperature



BST–SW UVLO Threshold



TGSR–TGSL UVLO Threshold



PIN FUNCTIONS

REG (Pin 3): Output of REG LDO. Power supply for gate drivers. Decouple this pin to ground with a minimum 4.7µF low ESR ceramic capacitor. Connect this pin to the external PMOS drain side.

BG1, BG2, BG3, BG4 (Pins 11, 10, 2, 1): Bottom Gate Driver Output. These pins drive the gates of the bottom N-channel MOSFETs. Voltage swing at these pins is from ground to REG.

BGBUF (Pin 12): Logic Output Pin. This pin is pulled up to REG when BGSH is at logic high, and it is pulled down to ground when BGSH is at logic low. For a slave LT8551, leave this pin floating. See the Applications Information section for more information.

TGBUF (Pin 13): Logic Output Pin. For a master LT8551, this pin is pulled up to REG voltage when (TGSH–TGSL) is at logic high, and it is pulled down to ground when (TGSH–TGSL) is at logic low. For a slave LT8551, leave this pin floating. See the Applications Information section for more information.

BST1, BST2, BST3, BST4 (Pins 14, 7, 6, 52): Boosted Floating Driver Supply. The (+) terminal of the boost-strap capacitor is connected to this pin. This pin swings from a diode voltage drop below REG up to V_{OUT} + REG.

TG1, TG2, TG3, TG4 (Pins 15, 8, 5, 51): Top Gate Driver Output. This is the output of a floating driver with a voltage swing equal to REG superimposed on the switch node voltage.

SW1, SW2, SW3, SW4 (Pins 16, 9, 4, 50): Switch Node. Voltage swing at these pins is from a diode voltage drop below ground to V_{OUT}.

TGSR (Pin 17): The Rail of Primary Channel Top Gate Sense Circuit. For a master LT8551, connect this pin to the primary channel top gate driver's boost node. This pin, combined with TGSH, TGSL pins, is to sense the primary channel top MOSFET's state. For a slave LT8551, connect this pin to REG.

TGSH (Pin 18): Input of Primary Channel Top Gate Sense Circuit. For a master LT8551, connect this pin to the primary channel top MOSFET's gate. This pin, combined with TGSR, TGSL pins, is to sense the primary channel top MOSFET's state. For a slave LT8551, connect this pin to the master LT8551's TGBUF pin.

TGSL (Pin 19): Lower Rail of Primary Channel Top Gate Sense Circuit. For a master LT8551, connect this pin to the primary channel top MOSFET's source. This pin, combined with TGSR, TGSH pins, is to sense the primary channel top MOSFET's state. For a slave LT8551, connect this pin to ground.

CLK1, CLK2 (Pins 21, 20): Clock Pin. These two pins are used to synchronize the primary channel to all other channels. See the Applications Information section for more information.

BGSH (Pin 22): Logic Input of Primary Channel Bottom Gate Sense Circuit. For a master LT8551, connect this pin to the primary channel bottom MOSFET's gate. This pin is to sense the primary channel bottom MOSFET's state. For a slave LT8551, connect this pin to the master LT8551's BGBUF pin.

SYNC (Pin 23): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must exceed 1.2V, and the low level must be less than 0.8V. Drive this pin to less than 0.8V to revert to the internal free-running clock. See the Typical Applications section.

PHS1, PHS2 (Pins 25, 24): Phase Selection Pin. These pins, combined with PHS3 and RT/MS, set the switching frequency and the phase of each channel. PHS1 and PHS2 are three-level input pins, they can be floated, set to REG or ground. When the PHS1/PHS2 is floating, add a 1nF cap from PHS1/PHS2to ground. See the Operation section for more information.

PIN FUNCTIONS

RT/MS (Pin 26): Timing Resistor Pin and Master Slave Selection Pin. This pin, combined with PHS1, PHS2 and PHS3, sets the switching frequency and the phase of each channel. Connecting a resistor to ground sets the chip as master LT8551. Connecting this pin to the REG pin sets the chip as slave LT8551. See the Applications Information section for more information.

ILIM (Pin 27): Maximum Current Sense Voltage Programming Pin. This pin is used to set the maximum sense voltage in the primary channel current sense amplifier and expanded channel current sense amplifier. It is a three level input pin. Connecting this pin to ground, REG or leaving it floating sets the maximum current sense voltage to 30mV, 60mV or 90mV, respectively. When the ILIM is floating, add a 1nF cap from the ILIM to ground.

ENOUT (Pin 28): For a master LT8551, this pin is an open-drain logic output pin. For a slave LT8551, it is an input pin. See more details in ENOUT Connection Section.

V_{CC} (Pin 29): Power Supply for Control Circuits. Decouple this pin to ground with a minimum 1µF low ESR ceramic capacitor. V_{CC} and REG need to be connected through a 1Ω resistor.

MODE (Pin 30): Stage Shedding Selection Pin. Connecting this pin to GND disables stage shedding feature. See the Operation section for more information.

$\overline{SHDN}$ (Pin 31): Shutdown Pin. This pin is used to enable/disable the chip. Drive below 0.3V to disable the chip. Drive above 1.2V (typical) to activate the chip. Do not float this pin.

IAMPN (Pin 32): For a master LT8551, connect this pin to local ground. For a slave LT8551, connect this pin to the master LT8551's IAMPN. See the Applications Information section for more information.

IAMPP (Pin 33): For a master LT8551, this is an output pin. It is the buffered signal of the Primary Channel Current Sense Amplifier output. For a slave LT8551, this is an input pin. When multiple LT8551 devices are used, connect all IAMPP pins together. See the Applications Information section for more information.

ISP (Pin 35): Primary Channel Current Sense Amplifier Input. The (+) input to the current sense amplifier is normally connected to DCR sensing network or current sensing resistor. This pin is only used for a master LT8551. Ground this pin for a slave LT8551.

ISN (Pin 34): Primary Channel Current Sense Amplifier Input. The (–) input to the current sense amplifier is normally connected to DCR sensing networks or current sensing resistors. This pin is only used for a master LT8551. Ground this pin for a slave LT8551.

REGSNS (Pin 40): REG LDO Voltage Sense Pin. Connect this pin to the primary channel gate driver power supply pin.

PHS3 (Pin 41): Phase Select Pin. This pin, combined with PHS1, PHS2 and RT/MS, set the switching frequency and the phase of each channel. PHS3 connects to REG or ground. See the Operation section for more information.

NC (Pin 42): No Connection. Leave this pin floating or connect to any adjacent pin.

ISN1, ISN2, ISN3, ISN4 (Pins 44, 36, 45, 38): Expanded Channel Current Sense Amplifier (–) Input. The (–) input to the current sense amplifier is normally connected to DCR sensing network or current sensing resistor.

ISP1, ISP2, ISP3, ISP4 (Pins 43, 37, 46, 39): Expanded Channel Current Sense Amplifier (+) Input. The (+) input to the current sense amplifier is normally connected to DCR sensing network or current sensing resistor.

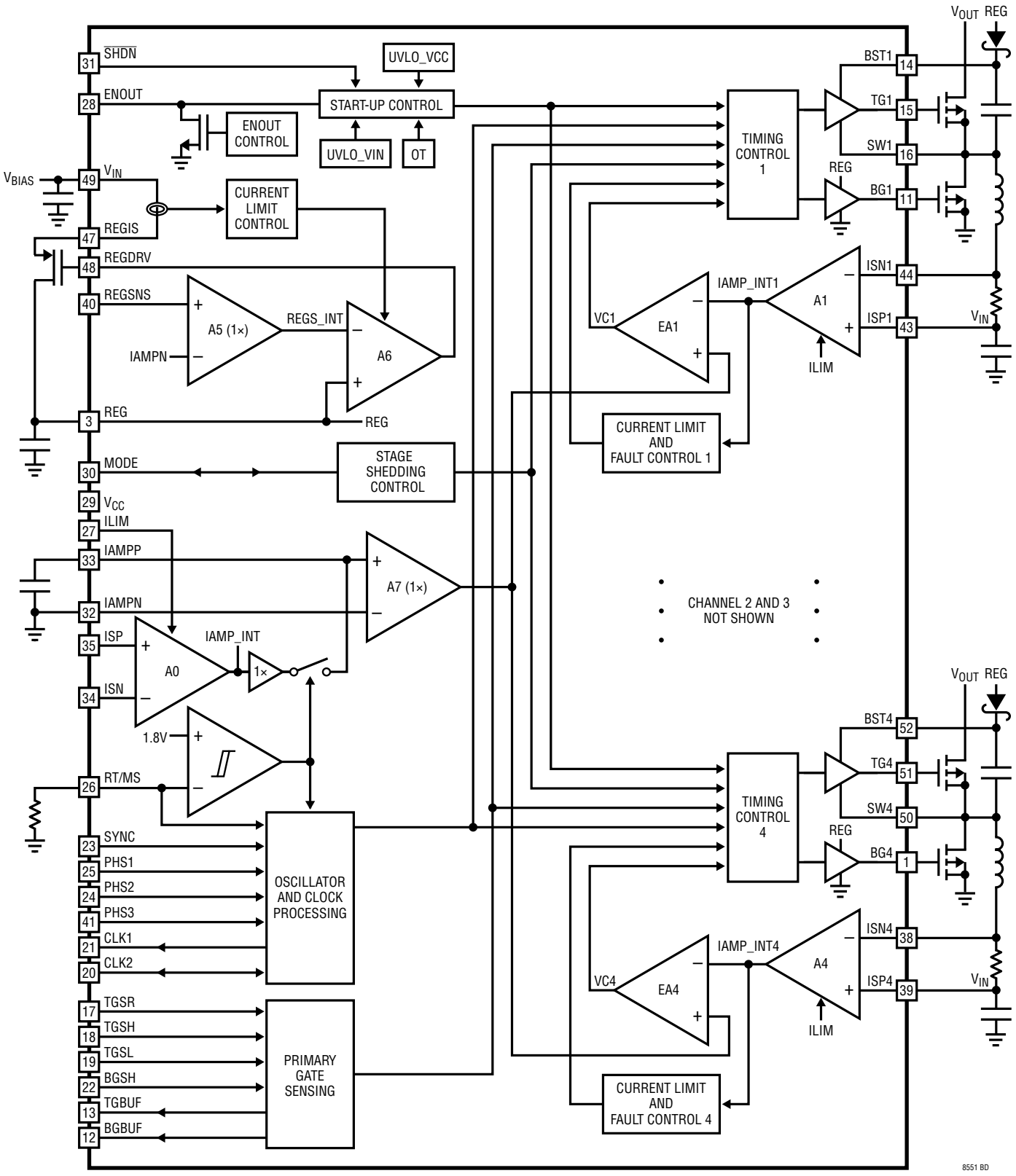
REGIS (Pin 47): REG LDO Current Sense Pin. Connect this pin to the external PMOS source side.

REGDRV (Pin 48): Gate Driver Output for REG LDO. Connect this pin to the external PMOS gate.

V_{IN} (Pin 49): Input Supply Pin. Must be locally bypassed to ground.

GND (Exposed Pad Pin 53/Pin 27): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM



OPERATION

Introduction

The LT8551 is a multiphase expander for synchronous boost controllers. Each LT8551, which has 8 gate drivers, can expand up to four phases. Multiple LT8551 devices can also be used together in a system, and up to 18 different phases can be supported. In addition, the part supports more than one phase per phase angle.

The ADI proprietary control architecture allows the LT8551 to cycle-by-cycle duplicate the operation of a boost controller (named as Primary Controller). The LT8551 measures the primary controller's inductor current as well as primary controller's gate driver operation timing, and at the same time, accurately monitors and adjusts the current of each expanded channel to achieve excellent DC and transient current sharing. The current sharing accuracy is ±6%, ±6% and ±10% over temperature when ILIM set at REG, Float and GND, respectively.

In normal operation, the primary boost regulator's switch current is compared with the expanded channel's switch current by the EA (EA1/2/3/4 in the Block Diagram). When the primary channel's current increases, the VC (VC1/2/3/4 in the Block Diagram) voltage also increases, which in turn controls the expanded channel's switches to increase the current until the expanded channel's current matches the primary channel's current.

System with Multiple LT8551 devices

One LT8551 can expand up to four channels. This configuration can provide enough power for most high current applications. However, for even higher power applications, the LT8551 can be configured for multi-chip operation. When two or more LT8551 devices are used together in a system, one LT8551 is the master and other LT8551 devices are slaves. Connecting a resistor from the RT/MS pin to ground sets the chip as the master and connecting the RT/MS pin to REG sets the chip as a slave. When only one LT8551 is used in a system, this LT8551 needs to be set as a master.

Stage Shedding Mode

The MODE pin is dedicated for the Stage Shedding feature. The MODE pin is an output pin for a master LT8551, and it is an input pin for a slave LT8551.

For a master LT8551, when the MODE pin is floating, the LT8551 operates in Stage Shedding mode at light loads. In this case, when the (ISP–ISN) peak voltage is lower than a certain value for some period of time, the part turns off channels 1 and 3 to increase overall efficiency. After channel 1 and 3 are off, if the (ISP–ISN) peak voltage is still lower than a certain value for some period of time, the part also turns off channel 4 and only leaves channel 2 running. For bidirectional applications, stage shedding should be disabled when the current is regulated in the reverse direction. Driving the MODE pin below 0.5V disables the Stage Shedding feature.

In a multiple LT8551 devices system, all chips' MODE pins need to be connected together and leave them floating if the Stage Shedding feature is desired. The master LT8551 senses the (ISP–ISN) voltage to decide the proper operation. The slave LT8551 devices follows the master LT8551's Stage Shedding operation with some delay. Driving all chips' MODE pins below 0.5V disables the Stage Shedding feature.

Clock Scheme

This section discusses the LT8551's clock scheme for a multiple LT8551 system. This clock scheme can easily apply to a single LT8551 system by ignoring the slave LT8551 devices.

A master LT8551 generates two clock signals: CLK1 and CLK2. In a multiple LT8551 system, as shown in Figure 1, all LT8551 devices' CLK2 pins need to be connected together. The CLK1 signal is at the fundamental switching frequency (Refer to Internal Oscillator and SYNC Pin and Clock Synchronization sections for more information), and it is used to synchronize the primary boost controller

OPERATION

and the slaves (in Figure 1). Under normal operation, the CLK2 frequency is at the CLK1 frequency times the total distinct phase number (TDPN), as shown in Figure 2. The number shown above the CLK2 pulses in Figure 2 is called the phase angle number (PAN).

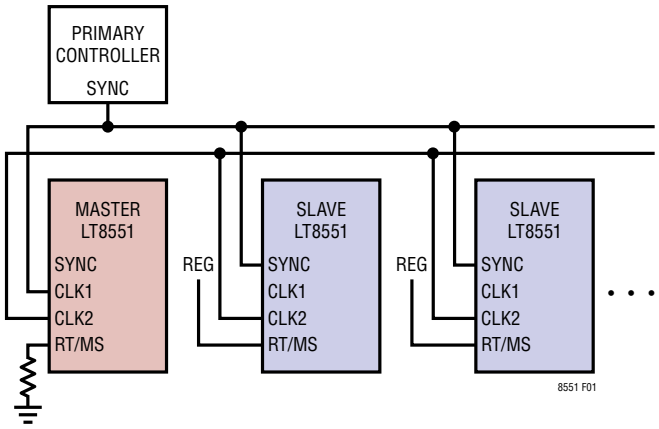


Figure 1. Clock Configuration in a Multiple LT8551 System

The total distinct phase number is programmed through the master LT8551's PHS1, PHS2 and PHS3 pins, according to Table 1. There is a delay locked loop in the chip which can force the primary controller's BG (Bottom Gate) rising edge to align with the pulse whose phase angle number equals the TDPN (in Figure 2).

Each expanded channel chooses one pulse from CLK2 in one CLK1 clock cycle. The rising edge of this chosen pulse aligns with the corresponding channel's bottom gate turn on edge with a very short delay. The master LT8551's channel 1 to channel 4 always choose the pulses whose phase angle number equals 1 to 4, respectively. Four channels of a slave LT8551 choose pulses with four consecutive phase angles. The phase angle number of the slave LT8551's channel 1 pulse is also programmed through PHS1, PHS2 and PHS3 pins, according to Table 1, and the pulses of the slave LT8551's channel 2, channel 3 and channel 4 have the next three phase angle number in succession. LT8551.

Table 2 shows the PHS1, PHS2 and PHS3 connections for a two LT8551 system with a total of 9 phases, including the primary controller's phase, as an example. The primary controller uses the CLK1 signal. The clocks used by the eight expanded channels are shown in Figure 3.

When the primary controller skips one or more pulses, the expanded channels also skip the same number of pulse(s). This function is realized by CLK2. As shown in Figure 4, when the primary controller skips one BG pulse, the CLK2 also skips a group of pulses with phase number from 1 to TDPN.

Table 1. Table for Programming Total Distinct Phase Number (TDPN) and Phase Angle Number (PAN)

PHS3	PHS2	PHS1	TDPN For Master	PAN of Slave Channel 1 Pulse
GND	GND	GND	NA	1
GND	GND	REG	2	2
GND	GND	Floating	3	3
GND	REG	GND	4	4
GND	REG	REG	5	5
GND	REG	Floating	6	6
GND	Floating	GND	7	7
GND	Floating	REG	8	8
GND	Floating	Floating	9	9
REG	GND	GND	10	10
REG	GND	REG	11	11
REG	GND	Floating	12	12
REG	REG	GND	13	13
REG	REG	REG	14	14
REG	REG	Floating	15	15
REG	Floating	GND	16	16
REG	Floating	REG	17	17
REG	Floating	Floating	18	18

Table 2. Design Example for a 9-Phase Application

	PHS3	PHS2	PHS1	PAN for Channel 1, 2, 3 and 4
Master LT8551	GND	Floating	Floating	1, 2, 3, 4
Slave LT8551	GND	REG	REG	5, 6, 7, 8

OPERATION

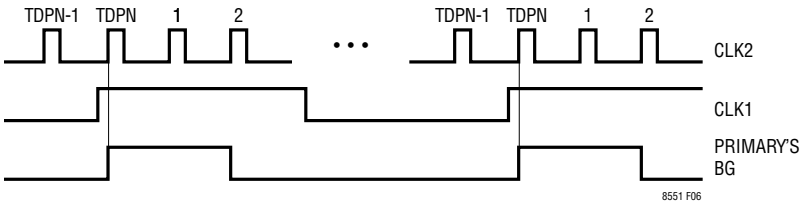


Figure 2. CLK1, CLK2 and Primary's BG

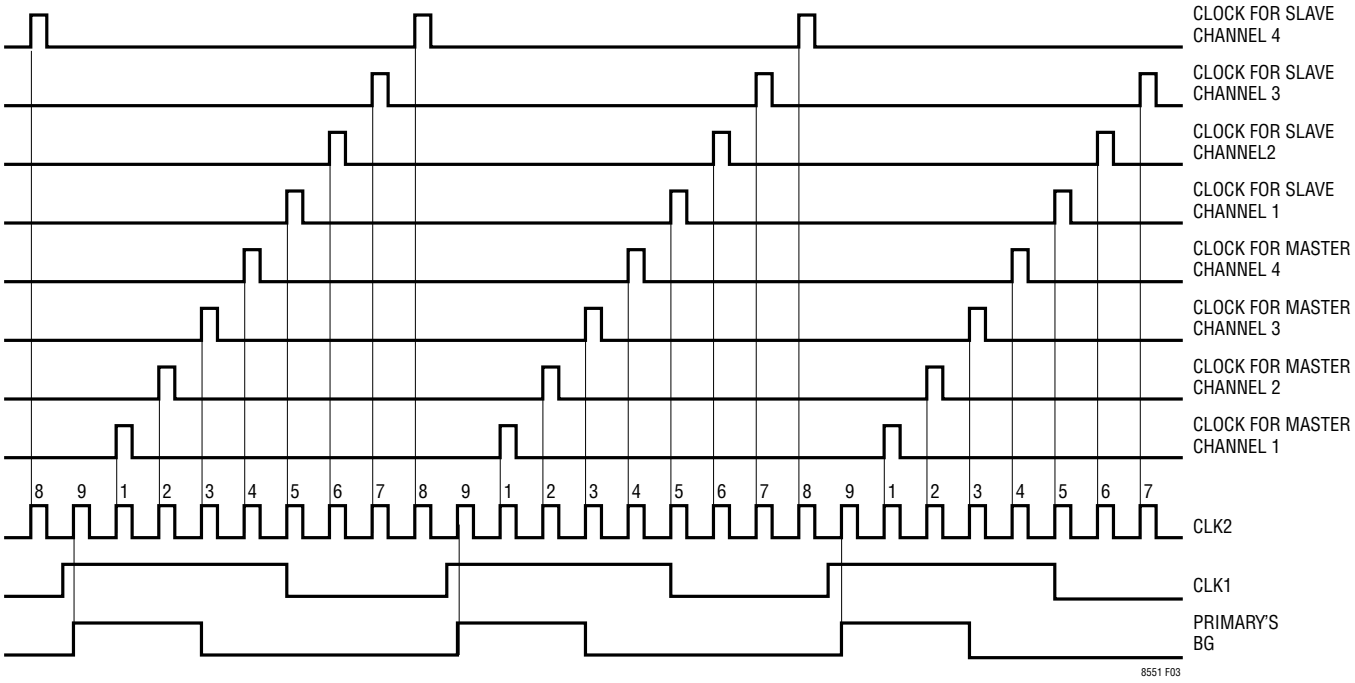


Figure 3. Clock Waveforms for a Two LT8551 System

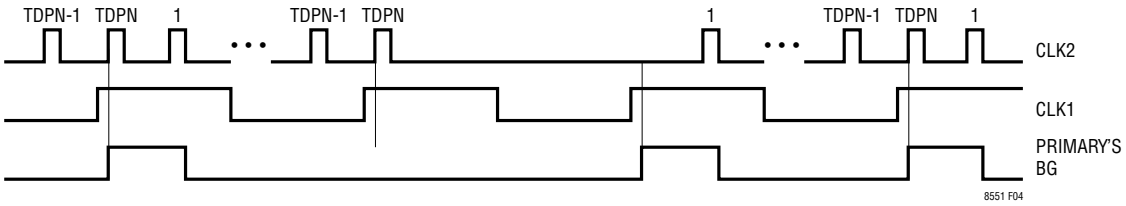


Figure 4. CLK1, CLK2 and Primary's BG Waveforms for Pulse Skipping

OPERATION

Primary Controller's Switch State Detection

This section discusses a system with multiple LT8551 devices. For a single LT8551 system, simply ignore the slave LT8551 devices in this discussion.

The primary controller's switch states are detected by the master LT8551, and this information is used by both master and slave LT8551 devices.

The primary controller's top switch state is sensed by the master LT8551's TGSR, TGSH, and TGSL pins, as shown in Figure 5. This floating top gate logic signal is converted to a ground based logic signal, and outputted to the TGBUF pin. The master LT8551's TGBUF is then connected to the downstream slaves' TGSH, as shown in Figure 5. The slave's TGSR and TGSL are connected to the REG and GND respectively. If the (TGSR–TGSL) voltage is less than 2.3V (typical), the TGBUF pin will be forced to ground for both of the master and slave LT8551. See the Applications Information section for more information.

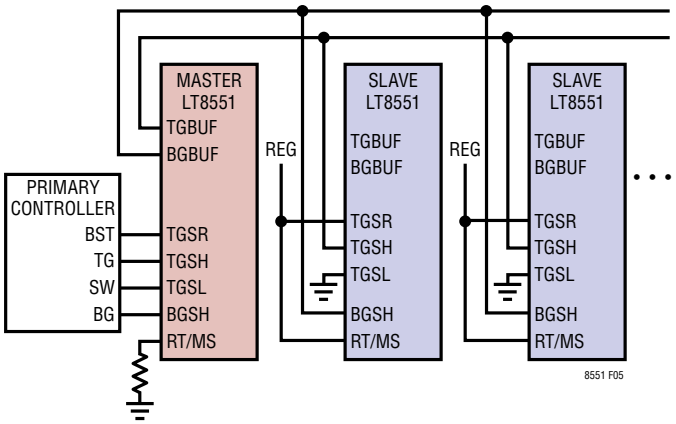


Figure 5. Gate Sensing in a Multiple LT8551 System

A similar method is used for the primary controller's bottom switch state detection, also shown in Figure 5. Since the primary BG is a ground based signal, only one pin (BGSH) is needed for the primary's BG detection. Since the master LT8551 passes the primary's switch states to the slaves, this avoids routing the primary's noisy BST, TG, SW and BG signals around the board.

Primary Controller's Inductor Current Sensing

This section discusses a system with multiple LT8551 devices. For a single LT8551 system, simply ignore the slave LT8551 devices in this discussion.

The primary controller's inductor current is detected by the master LT8551, and this information is used by both the master and slave LT8551 devices.

As shown in Figure 6, the primary controller's inductor current is detected by the master LT8551's ISP and ISN pins. This signal is amplified, and then outputted to the master LT8551's IAMPP pin. For stability purposes, a cap is required from the IAMPP to GND, and total capacitance must be between 100pF and 470pF. For a slave LT8551, the ISP and ISN pins are not used and should be grounded, and the IAMPP is an input pin. To pass the primary's inductor current information from the master LT8551 to the slave LT8551 devices, all LT8551 devices' IAMPP and IAMPN pins are connected together, respectively. Connect the IAMPN pins to the master LT8551's local ground. The IAMPP and IAMPN are connected to the inputs of a unity gain differential sense amplify (A7 in the Block Diagram). See the Applications Information section for more information.

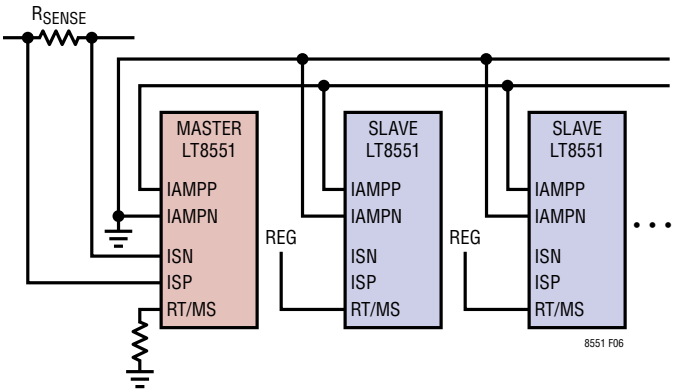


Figure 6. Primary Regulator's Switch Current Sensing in Multiple LT8551 System

The signal across the primary inductor current sense resistor is only tens of mV. By passing the amplified current signal from the master to the slaves, routing sensitive small signals around the board is avoided.

OPERATION

Current Sensing Gain, Limit and Fault

The gain of five current amplifiers (A0 to A4 in the Block Diagram) has three gain levels which are set by the ILIM pin. Connecting the ILIM pin to GND/REG/Floating sets the gain to 33.3/16.7/11.1, respectively. The outputs of these amplifiers are called IAMP_INT/IMAP_INTx (in the Block Diagram). The relation between the IAMP_INT/IAMP_INTx and the (ISP–ISN)/(ISPx–ISNx) are shown in Figure 7. There is a 1.4V offset. For expanded channels, the IAMP_INTx's value determines the current limit and current fault as shown in Figure 8.

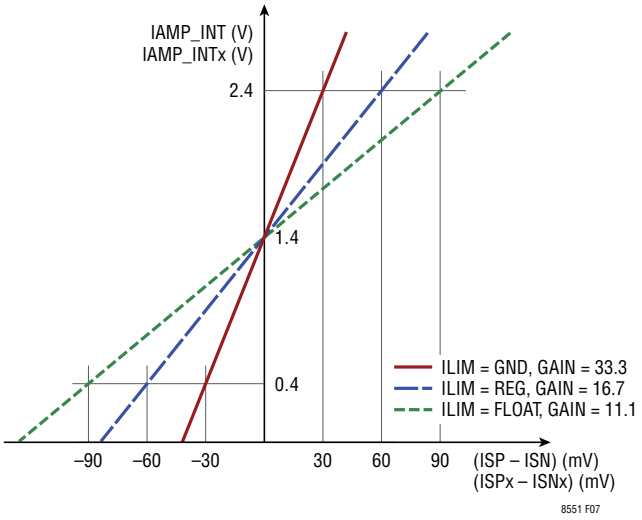


Figure 7. Current Sensing Amplifier Output Vs. Input at Three Different Gains

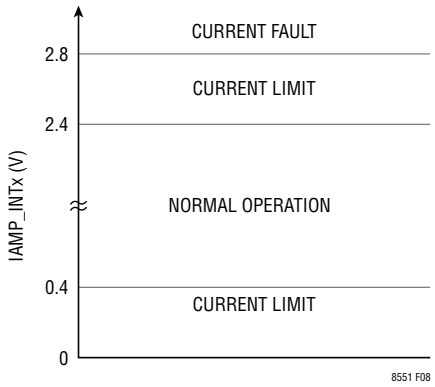


Figure 8. IAMP_INTx Voltage for Current Limit and Current Fault

When the IAMP_INTx reaches 2.4V but lower than 2.8V, or if it drops below 0.4V, the corresponding channel enters current limit. When the current limit condition is detected, both corresponding channel's BGx and TGx are pulled low immediately. The channel resumes switching at the next clock rising edge after the current limit condition is removed. The corresponding (ISPx–ISNx) voltages at current limit are indicated in Figure 7.

When the IAMP_INTx reaches 2.8V, the corresponding channel enters current fault. When the current fault condition is detected, the corresponding channel enters into a fault sequence which is described in more detail in the Fault Sequence section.

Shutdown and Start-Up

Figure 9 illustrates the start-up sequence for the LT8551. The shutdown pin for the chip is $\overline{\text{SHDN}}$. When it is driven below 0.3V, the chip is disabled (chip off state) and quiescent current is minimal. Increasing the $\overline{\text{SHDN}}$ voltage can increase quiescent current but will not enable the chip until $\overline{\text{SHDN}}$ is driven above 1.15V (typical) after which the REG LDO is enabled (switcher off state).

Starting up the switching regulator happens after VCC has risen above 3.55V (typical) and the ENOUT has been driven above 2.1V (typical). For a master LT8551, the ENOUT is an open drain pin. When VCC is lower than 3.55V, the ENOUT is pulled to GND to disable switching. For a slave LT8551, the ENOUT is always a high impedance input pin.

Fault Sequence

The LT8551 activates a fault sequence (see Figure 9) when IAMP_INTx is higher than 2.8V, which is the fault condition for a LT8551. The fault event is independent of channels, which means that the fault condition occurring in one channel won't directly affect other channels. If one of these conditions occurs for a certain channel, the corresponding channel's gate driver outputs are pulled low. If one of the LT8551's channels enters latch off mode (see Figure 9), only restarting the whole chip will reactivate the channel.

OPERATION

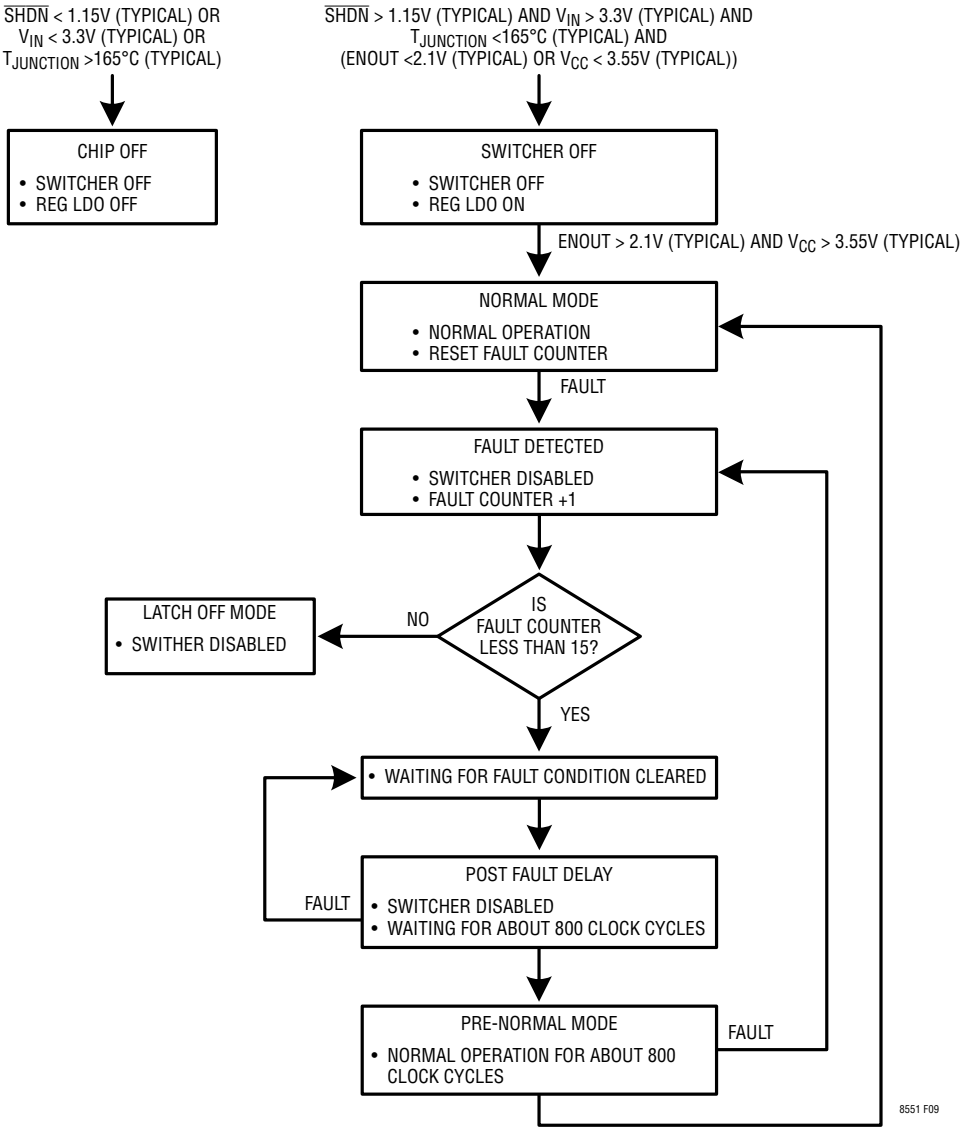


Figure 9. Start-Up and Fault Sequence

ENOUT Connection

For a master LT8551, this pin is an open-drain logic output pin. The master LT8551's ENOUT pin is pulled to ground when it is not ready for switching. For a slave LT8551, this pin is an input pin. For both master and slave LT8551 devices, when the ENOUT pin is lower than 2.1V (typical), the gate driver's switching activity is disabled.

When a master LT8551 is not ready for switching, it is desired to disable the primary controller and the slave LT8551 devices' switching activity. Figure 10 is one recommended configuration.

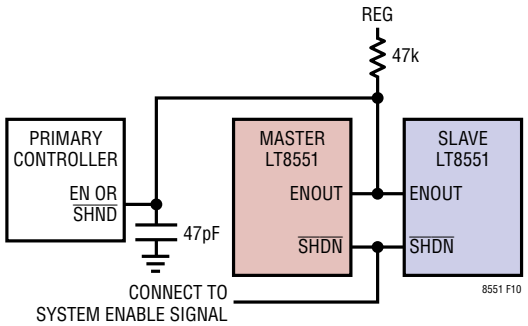


Figure 10. Recommended ENOUT Connection

APPLICATIONS INFORMATION

REG LDO and V_{CC} Power

The REG LDO supplies the power for the gate drivers and output stages of CLK1, CLK2, TGBUF and BGBUF. Once the $\overline{SHDN}$ pin is higher than 1.15V, REG will be regulated to 4V (typical), (REGSNS – IAMPN) voltage, or 5.25V (typical) from V_{IN}, depending on whether (REGSNS – IAMPN) is lower than 4V, or higher than 4V but lower than 5.25V, or higher than 5.25V respectively, as shown in Figure 11. The REG pin must be bypassed to power ground with an X5R or X7R ceramic capacitor of at least 4.7µF placed close to the REG pin.

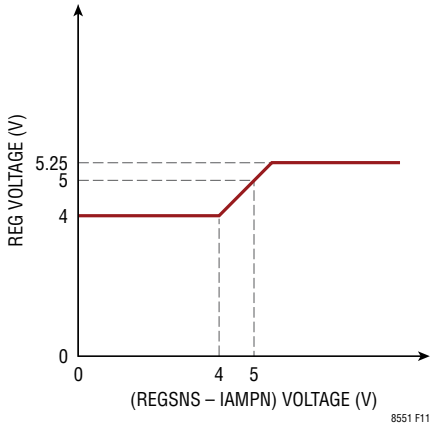
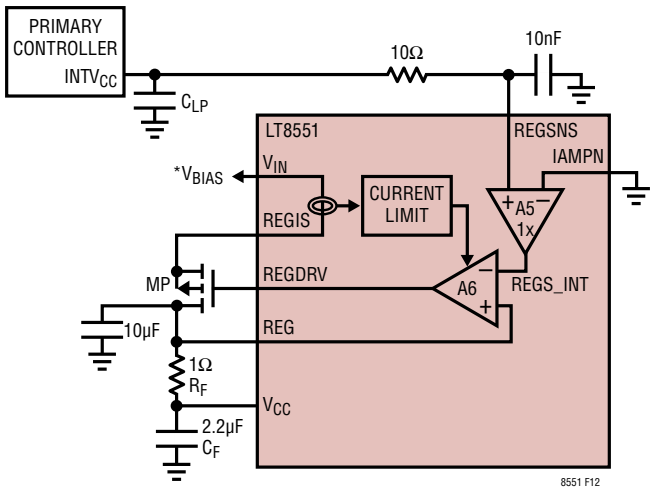


Figure 11. REG Voltage vs REGSNS Voltage

V_{CC} is the power supply for most of the internal circuitry and it's connected to REG through an external filter (R_F, C_F) to filter the switching noise in REG, as shown in Figure 12, the filter should be placed close to the V_{CC} pin, typical value of R_F = 1Ω, C_F = 1µF is recommended. The internal UVLO comparator disables the LT8551's switching activity when V_{CC} is lower than 3.55V (typical).

Primary $INTV_{CC}$ Sensing

The primary controller gate driver's power supply is $INTV_{CC}$, as shown in Figure 12. The primary $INTV_{CC}$ voltage is filtered and then sensed by the differential unity gain amplifier A5 in Figure 12, and buffered to REGS_INT as the reference voltage of the REG LDO. Notice that the (–) of A5 is connected to IAMPN. As has been discussed in the Primary Controller's Inductor Current Sensing section, both the master LT8551's IAMPN and the slave LT8551's IAMPN are connected to the master LT8551's local ground. Since the master's local ground and the primary controller's local ground may have small voltage difference, this can introduce a small error. To minimize this error, the master LT8551 should be placed close to the primary controller.



*LOWER VOLTAGE (V_{BIAS}) CAN BE USED FOR V_{IN} PIN TO REDUCE THERMAL STRESS INSTEAD OF USING THE SUPPLY FOR THE POWER STAGE

Figure 12. REG LDO Configuration

REG LDO Current Limit and External Power PMOS Selection

Overcurrent protection circuitry limits the maximum current drawn from the REG LDO. When the V_{CC} voltage is below 3.3V during start-up or an overload condition, the typical current limit is about 110mA. When the REG voltage is higher than 3.55V, the current limit depends on the V_{IN} voltage as shown in Figure 13. If the V_{IN} voltage is lower than 13.6V or higher than 30V, the current limit is about 220mA or 100mA respectively. If the V_{IN} voltage is between 13.6V and 30V, the current limit is inversely proportional to the V_{IN} voltage to limit the maximum power dissipation in the external power PMOS. The power dissipation in the external PMOS can be calculated by:

$$P = (V_{BIAS} – REG) \bullet I_{LDO}$$

Where V_{BIAS} (V_{IN} pin voltage) is the chip power supply for the LT8551, I_{LDO} is the current drawn from the REG LDO for a specific application. Use the following formula to calculate the junction temperature of the PMOS and

APPLICATIONS INFORMATION

compare the calculated value of T_J to the manufacturer's data sheets to help choose the appropriate PMOS that will not overheat.

$$T_J = T_A + P \bullet R_{TH(JA)} \quad (1)$$

Where:

T_J is the junction temperature of the PMOS

T_A is the ambient air temperature

P is the power dissipation of the PMOS.

$R_{TH(JA)}$ is the MOSFET's thermal resistance from the junction to the ambient air. Refer to the manufacturer's data sheets.

To reduce the power dissipation in the external PMOS, it's helpful to power up the chip with a lower voltage aux power supply (V_{BIAS}) instead of sharing the same power supply with the power stage, especially in a high input voltage application. Large enough copper area on the PC board is needed for the PMOS to alleviate thermal stress.

To ensure the loop stability, it's also recommended to choose a PMOS with Qg < 40nC.

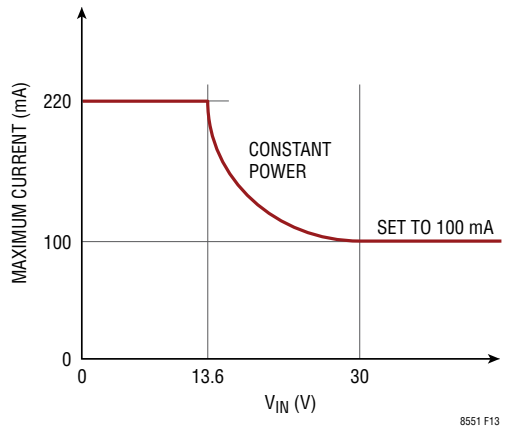


Figure 13. REG LDO Current Limit vs V_{BIAS} Voltage

Operating Frequency Selection

The expander system (primary controller and LT8551 devices) adopts a constant frequency ranging from 100kHz to 1MHz determined by the master LT8551. The primary controller and slave LT8551 devices are synchronized to the master LT8551 by connecting the master LT8551's CLK1 pin to their SYNC pins as shown in Figure 1. To minimize noise, it is recommended to add an RC filter between master CLK1 and each primary's or slave's SYNC pin. This RC filter should be close to SYNC pins with typical value of R = 10Ω, C = 220pF.

The frequency can be set either by the internal oscillator, or can be synchronized to an external clock source. A trade-off between efficiency and component size exists in selecting the switching frequency. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires more inductance and/or capacitance to maintain low output ripple voltage. The switching frequency can be set by placing an appropriate resistor from the RT/MS pin to ground and tying the SYNC pin low or high. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Internal Oscillator

The free-running switching frequency of the master LT8551 can be set using the internal oscillator by tying a resistor from RT/MS pin to ground while the SYNC pin is driven low (<0.8V) or high (>1.2V). The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{25{,}000}{R_T + 0.15}\text{kHz} \quad (2)$$

Where f_{OSC} is in kHz and R_T is in kΩ. Conversely, R_T (in kΩ) be calculated from the desired frequency (in kHz) using:

$$R_T = \frac{25{,}000}{f_{OSC}}\text{k}\Omega - 0.15\text{k}\Omega \quad (3)$$

APPLICATIONS INFORMATION

SYNC Pin and Clock Synchronization

The LT8551 has a phase-locked loop (PLL) to synchronize the internal oscillator to the external clock signal. The PLL is an edge sensitive digital type that provides zero degree phase shift between the external clock and internal oscillators.

To synchronize to an external clock source properly, the frequency of the external clock source must meet two criteria listed below:

1. The PLL is guaranteed to work properly only when the frequency of the external clock source ranges from 125kHz to 1MHz.
2. The external clock can be synchronized to only when it's faster than the free-running frequency set by the RT resistor. If the external clock is lower than f_{OSC}, as set by RT, the internal oscillator will oscillate at f_{OSC}.

Primary Controller Gate Sensing Filters and Dividers

As has been discussed in the Operation section, the primary controller's top and bottom switch states are detected by the master LT8551 gate sensing pins (i.e. TGSR, TGSH, TGSL and BGSH). This sensed top gate signal and bottom gate signal are buffered to the master LT8551's TGBUF and BGBUF respectively.

Since the primary controller's SW node moves fast, an RC filter R_F, C_F and bypass capacitor C_H must be used, as shown in Figure 14, to avoid falsely sensing the primary controller's top MOSFET's state. Optional Schottky clamps close to the TGSL pin of the LT8551 are recommended to prevent the TGSL pin from ringing below ground or exceeding the pin's absolute maximum rating if long traces are used to sense the top gate. Optional filters are also recommended for both of the primary controller's bottom gate sensing and the slave LT8551 devices' gate sensing pins, as shown in Figure 14. The time constant of these filters should be less than 30ns, typical values of R_F = 20Ω, C = 1nF are recommended.

The LT8551 is recommended to work with a primary controller which has gate driver rail lower than 5.5V. If the primary has higher than 5.5V gate driver rail, resistor

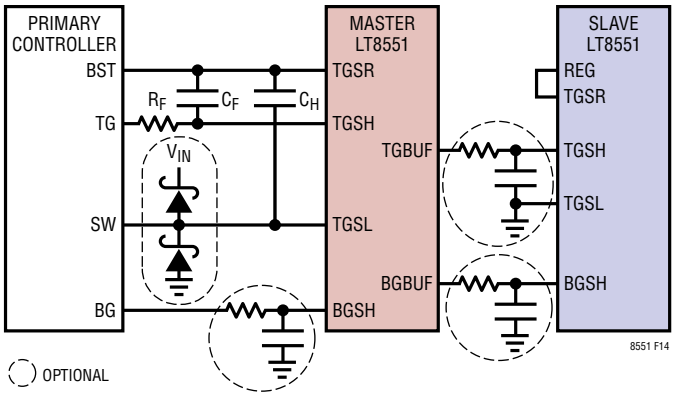


Figure 14. Gate Sensing Configuration with Filters and Schottky Clamps on TGSL

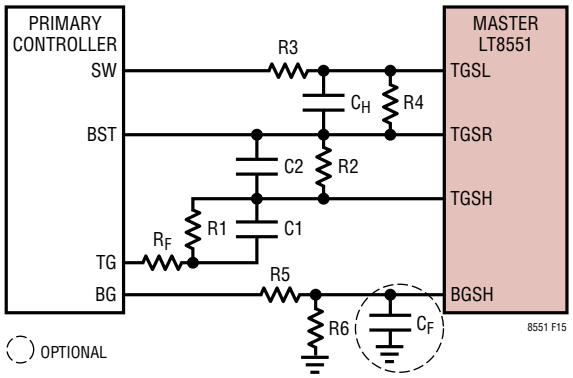


Figure 15. Gate Sensing Configuration when Primary Gate Driver Rail is Higher than 5.5V

dividers are required as shown in Figure 15. Use the following equations to design the adequate divider and filter for the gate sensing or refer to Table 3 for the recommended values:

$$\frac{R_F C1C2}{C1+C2} \leq 30ns$$

$$\frac{C_F R5 R6}{R5+R6} \leq 30ns$$

$$\frac{R2}{R1+R2} = \frac{R4}{R3+R4} = \frac{R6}{R5+R6} = \frac{5.5V}{\text{Primary's } V_{INTVCC}}$$

$$R1C1 = R2C2$$

APPLICATIONS INFORMATION

Table 3. Recommended Values for Gate Sensing Filters

Primary's $INTV_{CC}$ Voltage (V)	R1 = R3 = R5 (kΩ)	R2 = R4 = R6 (kΩ)	C1 (nF)	C2 (nF)	R_F (Ω)
6.0	4.7	47	10	1.0	22
6.5	10	33	3.3	1.0	27
7.0	10	22	2.2	1.0	30
7.5	10	15	1.0	0.68	47
8.0	10	15	1.0	0.68	47
9.0	10	13	1.0	0.68	47
9.5	9.1	13	1.0	0.68	47
10	10	10	1.0	1.0	43

In addition, R1–R6 should be in the range of kΩ or higher to reduce the quiescent current. And in order to sense the primary top gate state correctly during the SW node transition, the C1 and C2 capacitance within 1nF to 100nF and C_H>4.7nF are recommended. These dividers and filters should be close to the master LT8551 in the PCB layout.

Power Stage Components Selection Guideline

The power stage components include the input and output capacitor, inductor, power N-channel MOSFETs and the optional Schottky diode. Each LT8551's expanded channel always adopts the exact same power stage components as the primary controller. The following sections offer a brief guideline for the power device selection. Refer to the primary controller's data sheet for more detailed information.

Inductor Selection

For high efficiency, choose an inductor with low core loss, such as ferrite. Also the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

The inductor selection is interrelated with maximum average load current and inductor current ripple, which means the inductor must have a rating greater than its peak operating current to prevent saturation and the inductance must be large enough to decrease the current ripple so that the maximum average current can be fed to the load due to the limited peak inductor current.

Power MOSFET, Schottky Diode (Optional) Selection and Efficiency Considerations.

Critical parameters for power MOSFET selection include the on-resistance ($R_{DS(ON)}$), Miller capacitance (C_{MILLER}), BV_{DSS} (i.e. drain-source breakdown voltage) and maximum output current, all those parameters can be found on the manufacture's data sheet. The gate drive voltage is set by the REG LDO (5V, typical value), consequently logic level (5V) MOSFET must be used for the LT8551.

It's very important to consider power dissipation when selecting the power MOSFETs. The most efficient circuit will use MOSFETs that dissipate the least amount of power. Power dissipation must be limited to avoid overheating that might damage the device. When the LT8551 operates in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is $I_{OUT(MAX)}$ the MOSFET power dissipation at maximum output current is given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet I_{OUT(MAX)}^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low.

APPLICATIONS INFORMATION

The term (1+ δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

Based on the power dissipation, the MOSFET junction temperature can be obtained using the formula (1) in the REG LDO Current Limit and External Power PMOS Selection section to pick an adequate MOSFET that will not overheat.

An optional Schottky diode in parallel with the top switch conducts during the dead time between the conduction of the main switch and the synchronous switch. This prevents the body diode of the synchronous switch from turning on, storing charge and requiring a reverse recovery period that could reduce the overall efficiency. Although improving the efficiency, the Schottky diode also exhibits much higher reverse leakage current than the silicon diode particularly at high temperature, the combination of high reverse voltage and current can lead to self-heating of the diode. Choose a package with lower thermal resistance (θ_{JA}) to minimize self-heating of the diode.

C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk capacitance in a single phase boost converter is given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (e.g., OS-CON and POSCAP).

Topside MOSFET Driver Supply (C_{BX}, D_{BX})

An external bootstrap capacitor, C_{BX}, supplies the gate driver voltage for the top switch. This capacitor is connected between BSTx and SWx and is charged through Schottky diode DBX from REG when the SWx pin is low. When the top switch turns on, the SWx rises to V_{OUT} and the BSTx rises to V_{OUT} + REG. The boost capacitor needs to store about 100 times the gate charge required by the top switch. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The bypass capacitance from REG to GND should be at least ten times the bootstrap capacitor value. In addition, the reverse breakdown of the Schottky diode must greater than the maximum power V_{OUT} voltage.

Inductor Current Sensing

The LT8551 can be configured to sense the inductor current through either low value series current sensing

APPLICATIONS INFORMATION

resistor (R_{SENSE}) or inductor DC resistance (DCR). The choice between the two current sensing schemes is largely a design trade-off between cost, accuracy and power consumption. DCR is becoming popular since it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The ISPx/ISNx (i.e. ISP, ISP1/2/3/4, ISN, ISN1/2/3/4) pins are the inputs to the current sense amplifiers. The common mode input voltage range of the current sense amplifier is from 0V to 80V. The current sense resistor is normally placed at the input of the LT8551 in series with the inductor. Each ISPx pin also provides power to the current sense amplifier when ISPx is higher than 1.1V (typical). It draws 0µA to 100µA during normal operation. The ISNx pin current is less than 1µA. The high impedance ISNx input to the current amplifier allows accurate DCR current sensing.

Low Value Resistor Current Sensing: A typical R_{SENSE} inductor current sensing is shown in Figure 16a. The filter components (R_F, C_F) need to be placed near the LT8551. R_F values greater than 100Ω should be avoided as this may increase offset voltage. The filter time constant ($R_F \bullet C_F$) should be no more than 30nS. The positive and negative sense traces need to be routed as a differential pair close together and Kelvin (4-wire) connected underneath the sense resistor as shown in Figure 17. R_{SENSE} is chosen based on the maximum output current. Given the maximum input current, $I_{(MAX)}$, maximum sense voltage, $V_{SENSE(MAX)}$, and maximum inductor ripple current, $\Delta I_{L(MAX)}$, the value of the R_{SENSE} can be chosen from the following formula:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

I_{MAX} depends on the required output current $I_{OUT(MAX)}$ and can be calculated using:

$$I_{MAX} = I_{OUT(MAX)} \bullet \left(\frac{V_{OUT}}{V_{IN}} \right)$$

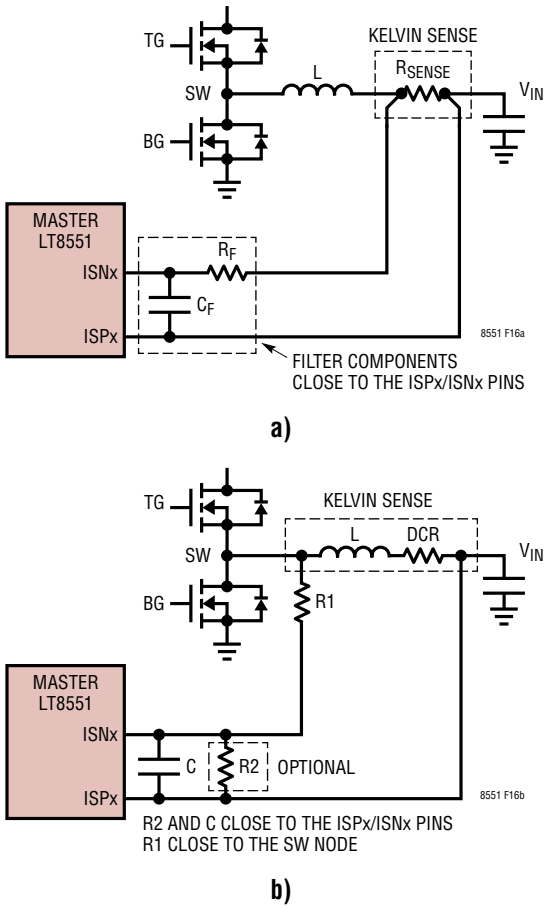


Figure 16. Inductor Current Sense Filter

DCR Inductor Current Sensing: For applications requiring the highest possible efficiency, the LT8551 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 16b. The DCR of the inductor represents the small amount of DC winding resistance, which can be less than 1mΩ for today's low value, high current inductors. In high current applications requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing. The inductor DCR is sensed by connecting an RC filter across the inductor. This filter typically consists of one or two resistors (R1 and R2) and one capacitor (C). If the external (R1||R2)•C time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across C will be:

$$V_{SENSE} = I_L \bullet DCR \bullet \frac{R2}{R1+R2}$$

APPLICATIONS INFORMATION

Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. With the ability to program the current limit through ILIM pin, R2 may be optional. C is usually selected in the range of 0.01µF to 0.47µF. This forces R1||R2 to be around kΩ range.

For DCR current sensing, the sense lines should also run close together to a Kelvin connection underneath the inductor as shown in Figure 17. To prevent noise from coupling into the sensitive small-signal nodes, resistor R1 should be placed close to the inductor, while R2 and C are placed close to the LT8551 as shown in Figure 16b.

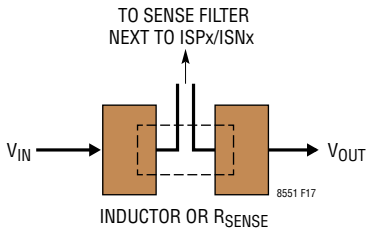


Figure 17. Sense Lines Placement for DCR Sensing or Resistor Sensing

Thermal Shutdown

If the die junction temperature reaches approximately 165°C, the LT8551 will go into thermal shutdown. All the power switches will be turned off. For a master LT8551, the ENOUT pin will be pulled down to ground so that it will shut down all the switching activity of the system. The LT8551 will be re-enabled when the die temperature has dropped by about 5°C (nominal).

Efficiency Considerations

The percent efficiency of LT8551 is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would lead to the most improvement. Percentage efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

Where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce power losses, several sources usually account for most of the losses in LT8551 circuits:

1. I^2R losses. I^2R losses arise from the DC resistance of the MOSFETs, inductor and current sense resistor. It is the majority of power losses at high input/output current. In continuous mode, the average input current flows through the inductor and R_{SENSE}, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the inductor's DCR, R_{SENSE} and the board traces to obtain I^2R losses.
2. Transition loss. This loss mostly arises from the brief amount of the time the bottom MOSFET spends in the saturation (Miller) region during the switching node transitions. It depends on the output voltage, load current, driver strength and MOSFET capacitance. The transition can be significant at high output voltages and low input voltage or high switching frequency.
3. REG current. This is the sum of MOSFETs driver and REG control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high then to low again, a packet of charge dQ moves from REG to ground. The resulting dQ/dt is a current out of REG that is typically much larger than control circuit current. In continuous mode, $I_{GATECHG} = f \bullet [Q_T + Q_B]$, where Q_T and Q_B are the gate charges of the top and bottom MOSFETs.

   As mentioned in the REG LDO and V_{CC} Power Section, powering up the REG LDO with lower power supply will not only improve efficiency, especially for high input voltage application, but also alleviate the thermal stress for the LDO's P-channel MOSFET.
4. Body diode conduction loss. During the dead time, the loss in the top/bottom MOSFET is $I_L \bullet V_F$, where V_F is around 0.7V. At higher switching frequency, the dead time becomes a good percentage of switching cycle and causes the efficiency to drop.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

APPLICATIONS INFORMATION

Circuit Board Layout Checklist

One recommended PC board design for a 9 phase system, primary controller and two LT8551 devices, is shown in Figure 18, the design can be expanded to more phases/channels if needed. Use the following general checklist to ensure the proper operation of the multiphase system:

- A multilayer PC board with dedicated ground planes is generally preferred to reduce noise coupling and improve heat sinking. The ground plane should be immediately next to the routing layer for the components (i.e. MOSFETs, inductors, sense resistors, input and output capacitors etc.)
- Keep small signal ground (SGND) and power ground (PGND)separate. Only one connection point between the SGND and PGND is required. It's desirable to return the SGND to a clean point on the PGND plane. Do not return the small signal components grounds to SGND through PGND. All power train components should be referenced to PGND. Use immediate vias to connect the power components to PGND. Several vias are needed for each power component.
- Place power components, such as C_{IN}, C_{OUT}, inductor and MOSFET, in one compact area. Use wide but shortest possible traces for high current paths (e.g. V_{IN}, V_{OUT}, PGND etc.) in this area to minimize copper loss.
- The BSTx/SWx nodes' voltage swings with a high dV/dt rate. These nodes are rich in high frequency noise components, and they are strong sources of EMI noise. To minimize the coupling between these nodes and other noise-sensitive traces, the copper area should be minimized. However, on the other hand, to conduct high inductor current and provide a heat sink to the power MOSFET, the SWx nodes PCB area cannot be too small. It's usually preferred to have a ground copper area placed underneath the SWx nodes to provide additional shielding.

  In addition to BSTx/SWx, the TGx and BGx are also high dV/dt signals, which must be routed away from the noise-sensitive traces. It is also highly recommended to use short and wide traces to route gate driver signals in order to minimize the impedance in gate driver paths. The TGx and SWx should be routed together with minimum loop area to minimize the inductance and high dV/dt noise. Likewise, the BGx should be routed close to a PGND trace, as shown in Figure 18. Try to route TGx, SWx, BGx traces on one layer only.

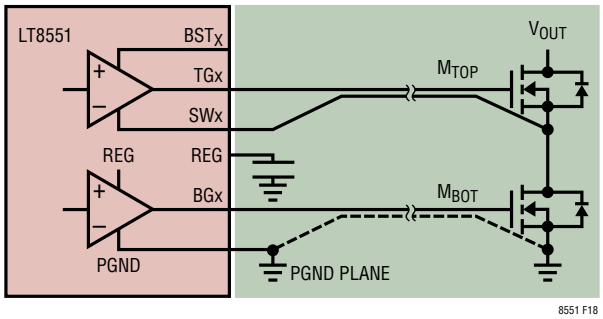
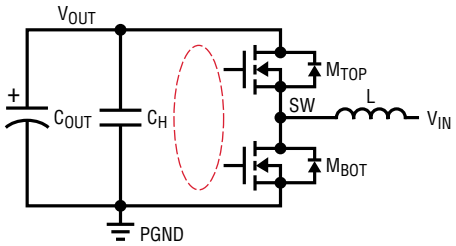
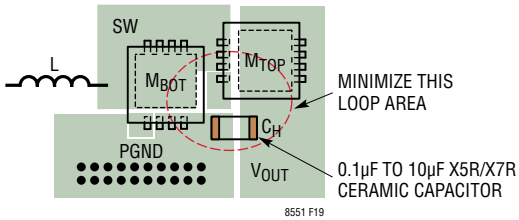


Figure 18. Gate Driver Routing Example

- Keep the high di/dt loop, which consists of the top MOSFET, bottom MOSFET, and the ceramic capacitor C_H as shown in Figure 19, as short as possible to minimize the pulsating loop inductance and absorb switching noise.



a) High di/dt Loop

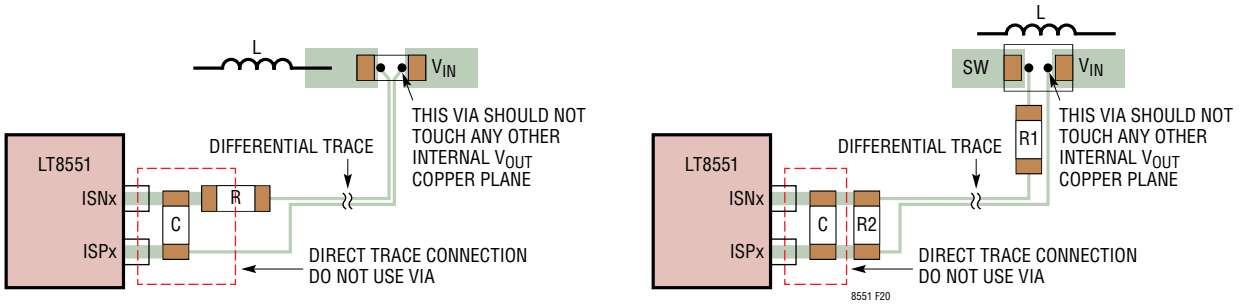


b) Recommended Layout Example

Figure 19. Minimize the High di/dt Loop Area in PCB Layout

APPLICATIONS INFORMATION

- The decoupling capacitors for REG, V_{CC}, V_{IN} and the current sense, etc. should be placed close to their pins, use PGND for the REG decoupling capacitor and SGND for V_{IN} and V_{CC} decoupling capacitors. To minimize the connection impedance, it's desired to connect the decoupling capacitors directly to the pins without using any via.
- Of all the small signal traces, current sensing traces are most sensitive to noise. The current sensing traces should be routed differentially with minimum spacing to minimize the chance of picking-up noise, as shown in Figure 20. In addition, the filter resistors and capacitors for current sensing traces should be placed as close to the ISPx/ISNx pins as possible. If the DCR sensing is used with an R/C network, the DCR sensing resistor R1 should be close to the inductor, while R2 and C should be close to the IC. Place the vias that connect the ISPx/ISNx lines directly at the terminals of the current sensing resistors or the inductors as shown in Figure 20.
- When routing the interface signals between a master LT8551, primary controller, and/or slave LT8551, keep the small-signal lines far from the noisy lines and shield these lines with a ground plane. A recommended line arrangement is shown in Figure 21.



a) Resistor Sensing **b) Inductor DCR Sensing**

Figure 20. Current Sensing PCB Design

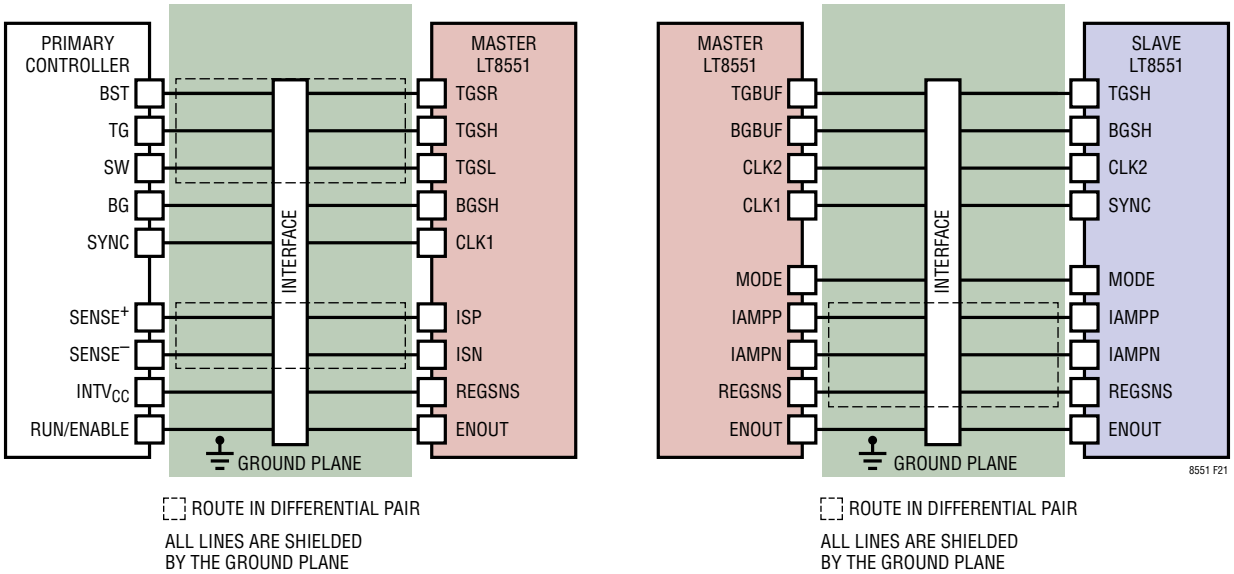
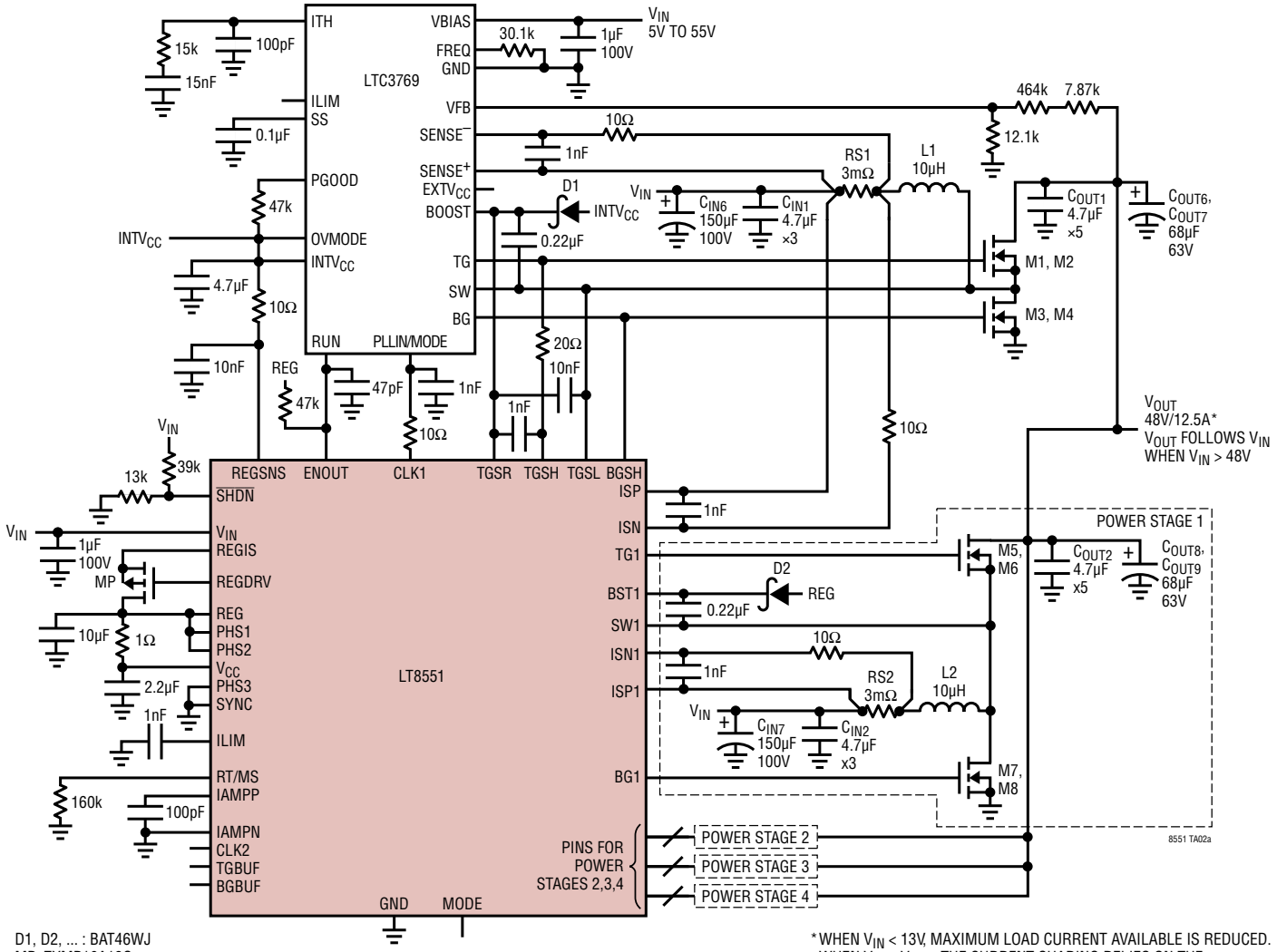


Figure 21. Recommended Signal Lines Arrangement for PCB

TYPICAL APPLICATIONS

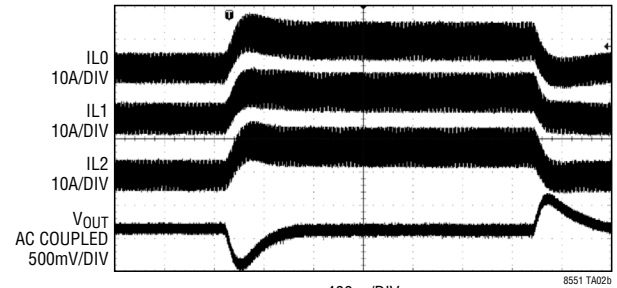
48V/12.5A Step-Up Expander System



D1, D2, ... : BAT46WJ
MP: ZXMP10A18G
RS1–RS5: PANASONIC ERJMB1SF3M0U
L1–L5: COILCRAFT SER2918H-103KL
C_{IN1}–C_{IN5}: TDK C3225X7S2A475M
C_{OUT1}–C_{OUT5}: TDK C3225X7S2A475M
C_{OUT6}–C_{OUT15}: PANASONIC EEHZC1J680P
M1, M2, M3, M4, M5, M6, M7, M8, ... : BSC100N06LS3

*WHEN V_{IN} < 13V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED. WHEN V_{IN} > V_{OUT}, THE CURRENT SHARING RELIES ON THE MATCHING OF THE $R_{DS(ON)}$ OF THE N-CHANNEL MOSFETS.

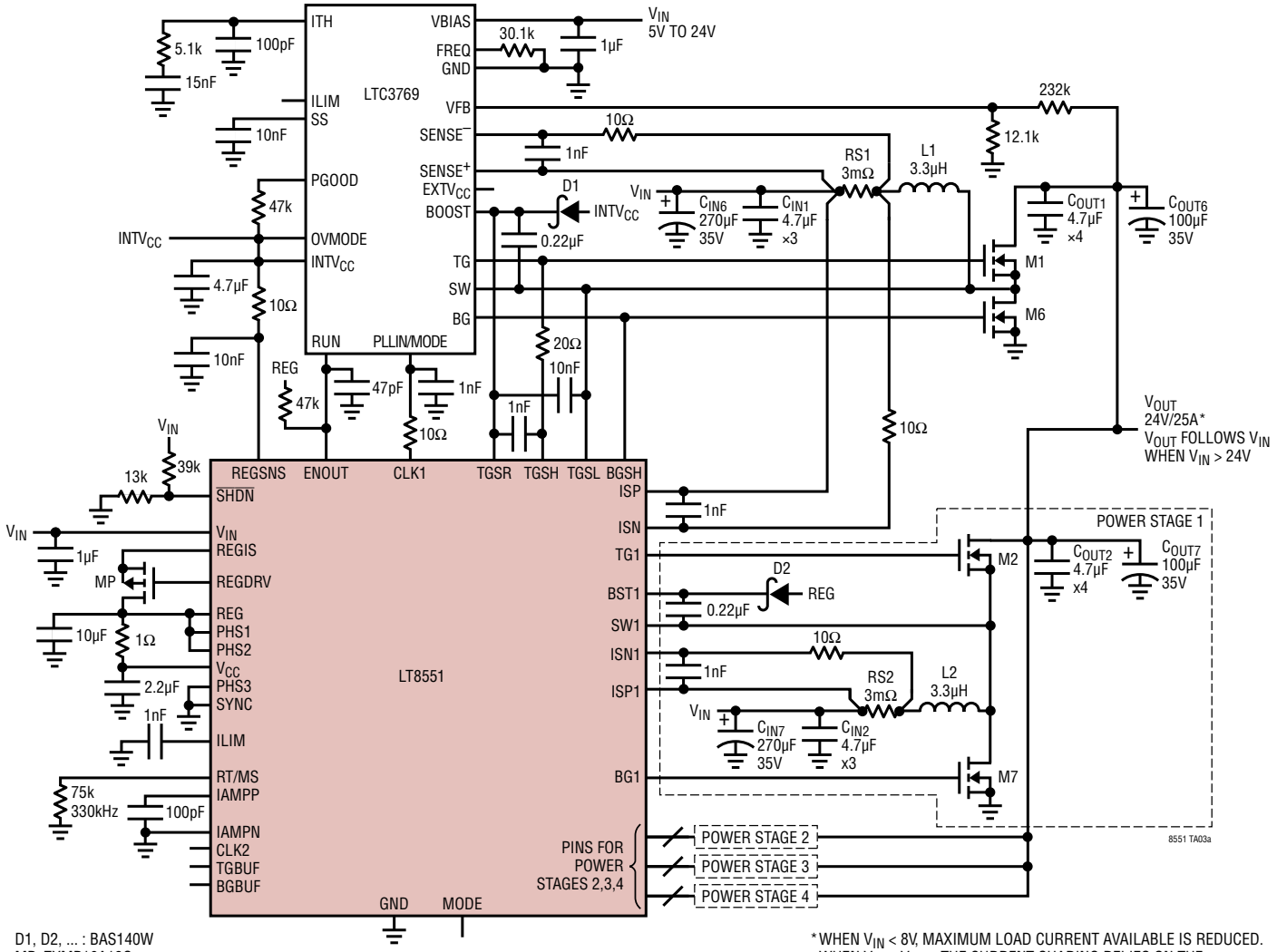
Load Step from 0A to 12.5A, V_{IN} = 16V, TDPN = 5



400µs/DIV

TYPICAL APPLICATIONS

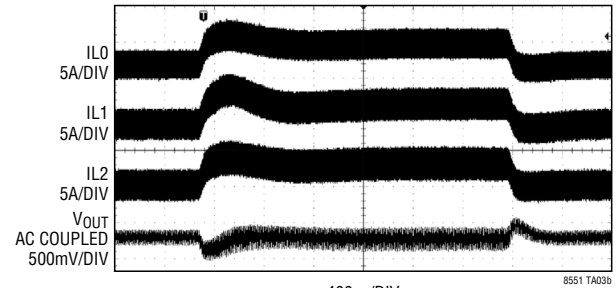
24V/25A Step-Up Expander System



D1, D2, ... : BAS140W
MP: ZXMP10A18G
RS1–RS5: PANASONIC ERJMB1SF3M0U
L1–L5: PULSE PA1494.362NL
C_{IN1}–C_{IN5}: TDK C2012X7R1V475K125AC
C_{IN6}–C_{IN10}: PANASONIC EEHC1V271P
C_{OUT1}–C_{OUT5}: TDK C2012X7R1V475K125AC
C_{OUT6}–C_{OUT10}: PANASONIC EEHZK1V101P
M1–M5: RENESAS RJK0453
M6–M10: RENESAS RJK0452

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED. WHEN V_{IN} > V_{OUT}, THE CURRENT SHARING RELIES ON THE MATCHING OF THE $R_{DS(ON)}$ OF THE N-CHANNEL MOSFETS.

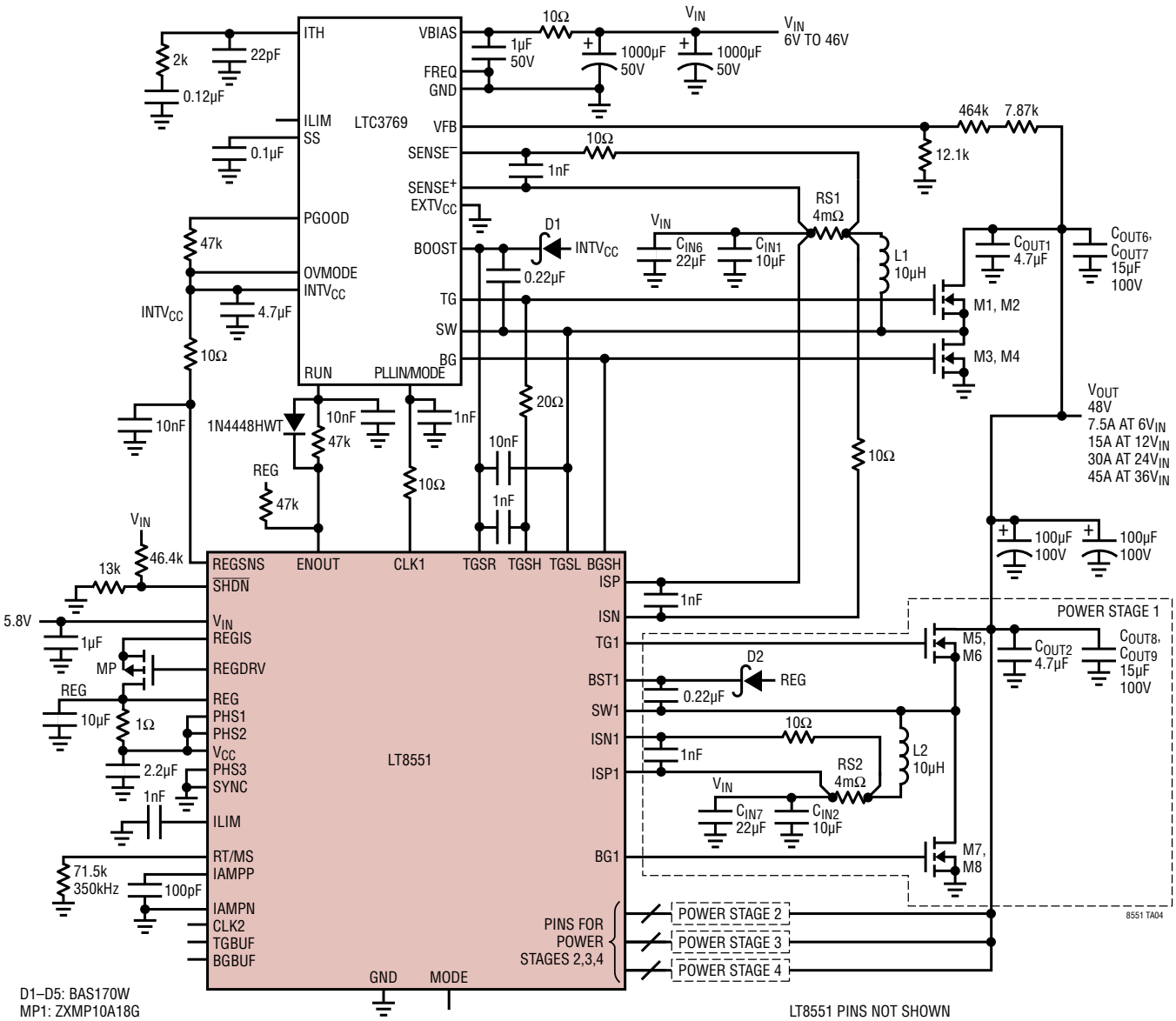
Load Step from 10A to 25A, V_{IN} = 18V, TDPN = 5



400µs/DIV

TYPICAL APPLICATIONS

48V Step-Up Expander System

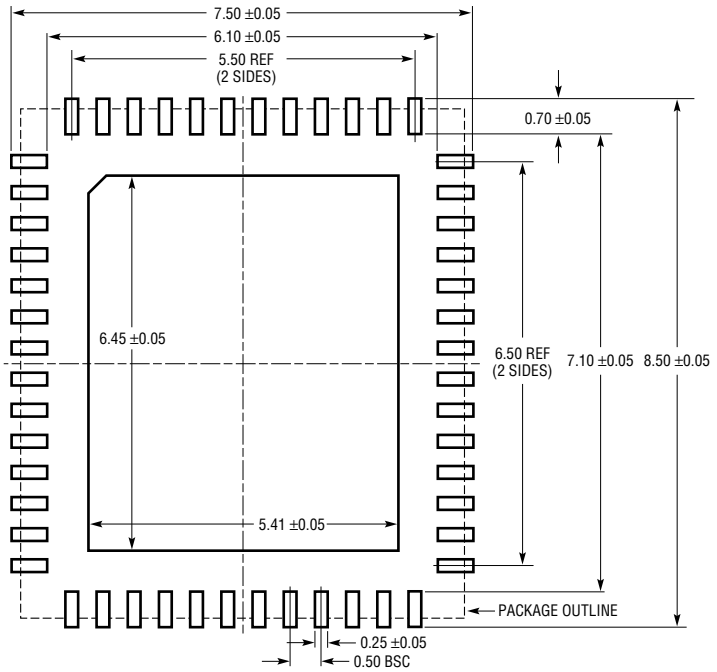


D1–D5: BAS170W
MP1: ZXMP10A18G
RS1–RS5: PANASONIC ERJ-MP4QF4M0U
L1–L5: COILCRAFT SER2918H-103KL
C_{IN1}–C_{IN5}: MURATA GRM32ER71H106KA12A
C_{IN6}–C_{IN10}: KRM55WR71H226MH01K
C_{OUT1}–C_{OUT5}: TDK C3225X7S2A475M200AB
C_{OUT6}–C_{OUT15}: KRM55WR72A156MH01K
M1–M20: BSC100N06LS3

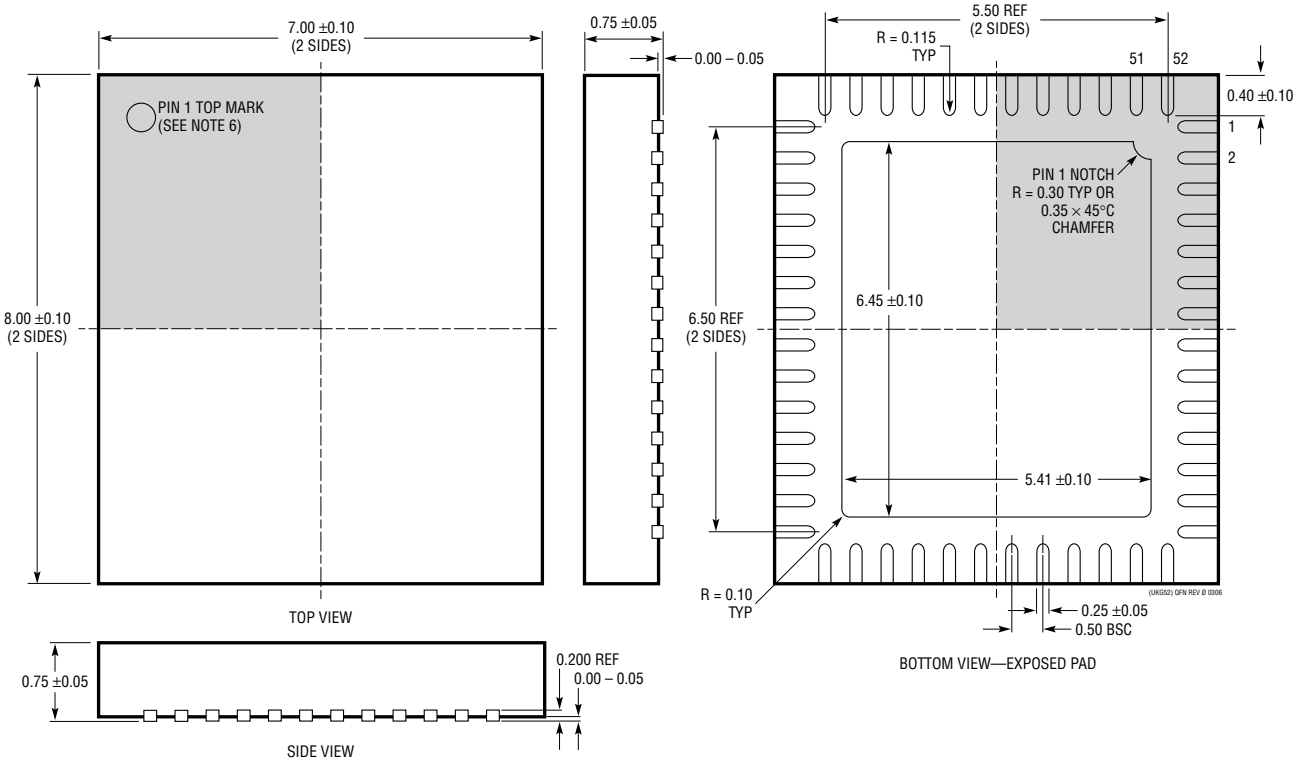
LT8551 PINS NOT SHOWN IN THIS CIRCUIT:
BST2, BST3, BST4
TG2, TG3, TG4,
SW2, SW3, SW4,
BG2, BG3, BG4,
ISP2, ISP3, ISP4,
ISN2, ISN3, ISN4

PACKAGE DESCRIPTION

UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)



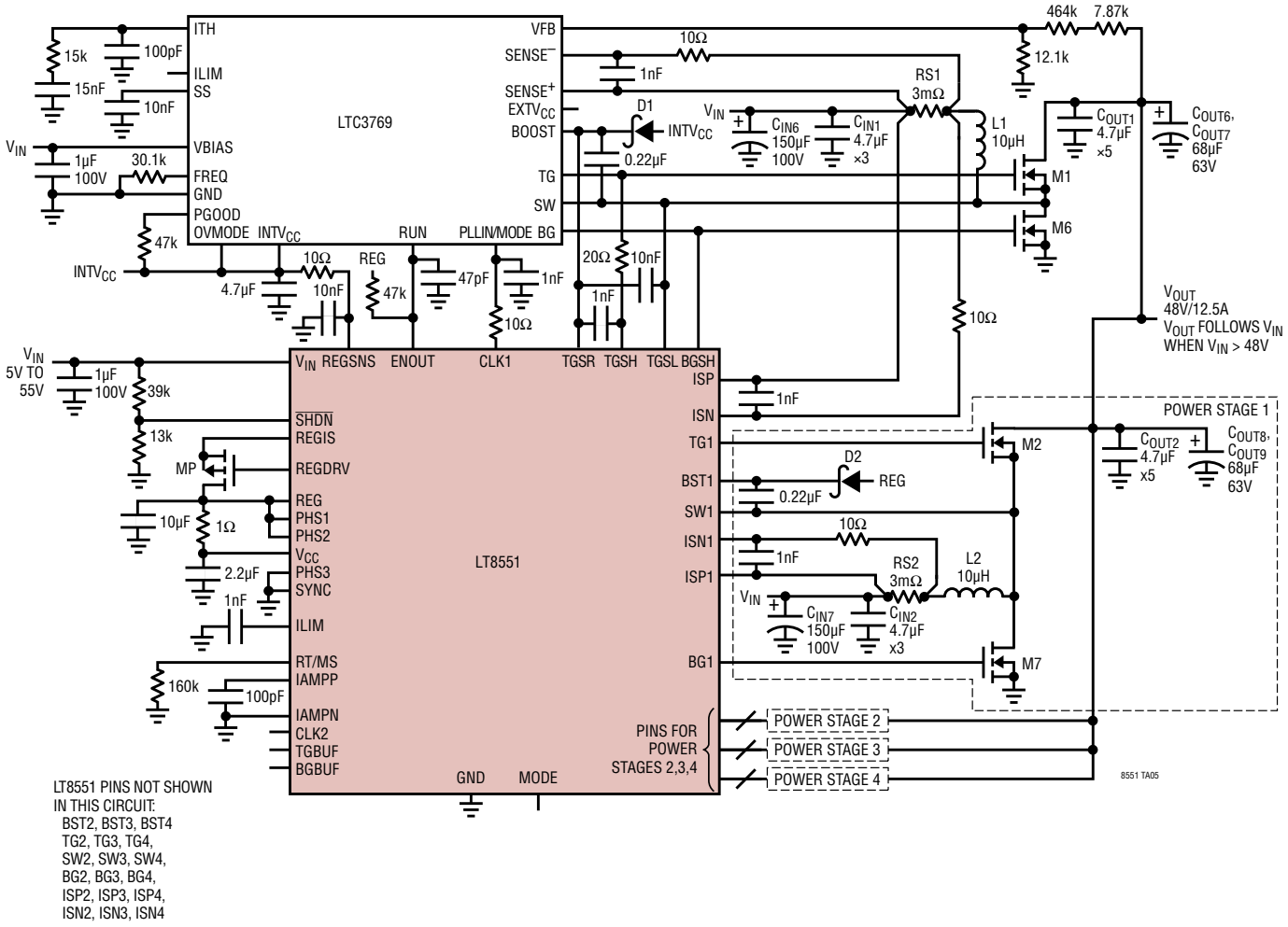
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

48V/12.5A Step-Up Expander System



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3786	38V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 3mm×3mm QFN-32, MSOP-16E
LTC3769	60V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.3V After Start-up) ≤ V_{IN}≤ 60V, V_{OUT} up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm×4mm QFN-24, TSSOP-20
LT8550	4-Phase Buck DC/DC Expander	V_{IN} up to 80V, 18 Distinct Phases, 125KHz to 1MHz, Supports Bidirectional Current Flow, 7mm×8mm QFN-52

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LT8551EUKG#PBF LT8551EUKG#TRPBF LT8551IUKG#TRPBF LT8551IUKG#PBF DC2332A-A DC2896A-B