

FEATURES

- Integrated fully differential ADC driver with signal scaling**
- Wide input common-mode voltage range**
- High common-mode rejection**
- Single-ended to differential conversion**
- ±2.048 V input range with 4.096 V REFBUF**
- Critical passive components**
- 0.005% precision matched resistor array for FDA**
- 9 mm × 9 mm, 0.80 mm pitch, 100-ball CSP_BGA package**
- 4× footprint reduction vs. discrete solution**
- Low power, dynamic power scaling, power-down mode**
- 143 mW typical at 15 MSPS**
- Throughput: 15 MSPS, no pipeline delay**
- INL: ±0.6 LSB typical, ±1 LSB maximum**
- SINAD: 89 dB typical at 1 kHz**
- THD: -115 dB at 1 kHz, -106 dB at 400 kHz**
- Gain error: 0.005%FS typical**
- Gain error drift: ±1 ppm/°C maximum**
- On-board reference buffer with VCMO generation**
- Serial LVDS interface**
- Wide operating temperature range: -40°C to +85°C**

APPLICATIONS

- ATE**
- Data acquisition**
- Hardware in the Loop (HiL)**
- Power analyzers**
- Nondestructive test (acoustic emissions)**
- Mass spectrometry**
- Travelling wave fault location**
- Medical imaging and instruments**
- Ultrasonic flow meters**

GENERAL DESCRIPTION

The ADAQ23875 is a precision, high speed, µModule® data acquisition solution that reduces the development cycle of a precision measurement systems by transferring the design burden of component selection, optimization, and layout from the designer to the device.

Using system-in-package (SIP) technology, the ADAQ23875 reduces end system component count by combining multiple common signal processing and conditioning blocks in a single device, solving many design challenges. These blocks include a low noise, fully differential analog-to-digital converter (ADC) driver (FDA), a stable reference buffer, and a high speed, 16-bit, 15 MSPS successive approximation register (SAR) ADC.

Using Analog Devices, Inc., iPassives® technology, the ADAQ23875 also incorporates crucial passive components with superior matching and drift characteristics to minimize temperature dependent error sources and to offer optimized performance (see Figure 1). The fast settling of the ADC driver stage, with fully differential or single-ended to differential input and no latency of the SAR ADC, provides a unique solution for high channel count multiplexed signal chain architectures and control loop applications.

The small footprint, 9 mm × 9 mm CSP_BGA package enables smaller form factor instruments without sacrificing performance. Single, 5 V supply operation is possible while achieving optimum performance from the device. The ADAQ23875 features a serial low voltage differential signaling (LVDS) digital interface with one-lane or two-lane output modes, allowing the user to optimize the interface data rate for each application. The specified operation of the µModule is from -40°C to +85°C.

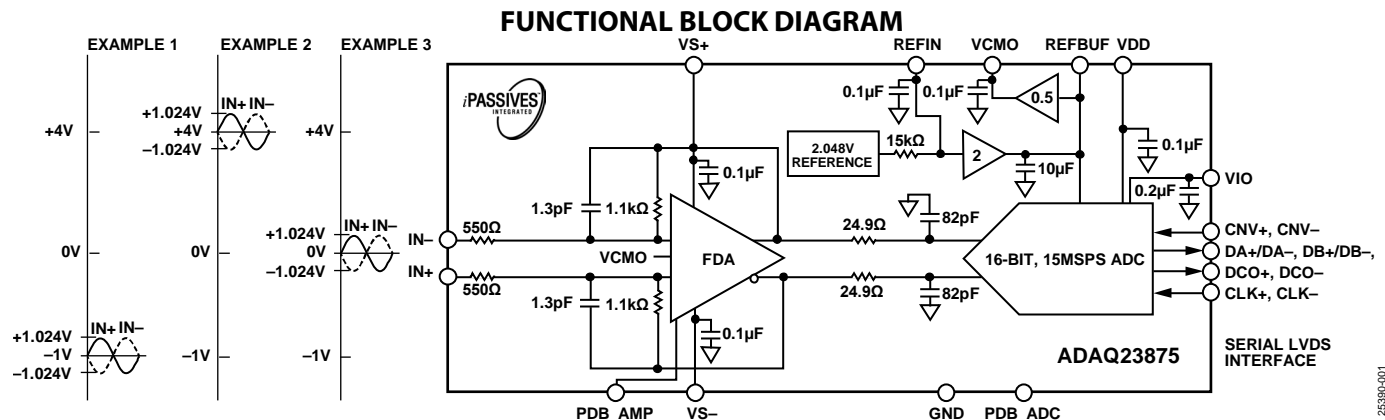


Figure 1. ADAQ23875 Configured for Gain = 2, ±2.048 V Differential Input Range

Rev. 0

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REVISION HISTORY

11/2020—Revision 0: Initial Version

SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS- = -1 V ± 5%, VS- = 0 V¹ (95% of VIN), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, sampling frequency (fs) = 15 MSPS, gain = 2, and all specifications TMIN to TMAX, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ²
RESOLUTION		18			Bits
ANALOG INPUT IMPEDANCE, ZIN	VIN = 4.096 V p-p Single-ended to differential configuration		550		Ω
	Differential configuration		1100		Ω
Input Capacitance	IN1+, IN1-		3.3		pF
Differential Input Voltage Range, VIN ³	Gain = 2, VIN = 4.096 V p-p	-2.048		+2.048	V
THROUGHPUT					
Complete Cycle		66.6			ns
Conversion Time		54	58	63	ns
Acquisition Phase ⁴			tCYC - 39		ns
Throughput Rate ⁵		0.02		15	MSPS
Transient Response ⁶	Full-scale step		52		ns
DC ACCURACY	Single-ended and differential configuration				
No Missing Codes		16			Bits
Integral Linearity Error		-1	±0.6	+1	LSB
		-12.5	±7.5	+12.5	ppm
Differential Linearity Error		-1	±0.25	+1	LSB
		-12.5	±3.125	+12.5	ppm
Transition Noise			0.73		LSBRMS
Gain Error		-0.045	±0.005	+0.045	%FS
Gain Error Drift		-1	±0.05	+1	ppm/°C
Offset Error		-1.5		+1.5	mV
Offset Error Drift		-1.8	±0.25	+1.8	ppm/°C
Common Mode Rejection Ratio (CMRR), Input Referred	ΔVICM/ΔVOSDIFF		96		dB
Power Supply Rejection Ratio (PSRR) Positive	VDD = 4.75 V to 5.25 V		105		dB
	VS+ = 4.75 V to 5.25 V, VS- = -1 V		115		dB
Negative	VS+ = +5 V, VS- = -0.75 V to -1.25 V		103		dB
1/f Noise ⁷	Bandwidth = 0.1 Hz to 10 Hz		9		μV p-p
Input Current Noise	f = 100 kHz		1		pA/√Hz
AC ACCURACY ⁸	Single-ended and differential configuration				
Dynamic Range	Input frequency (fIN) = 1 kHz, -60 dB input	88	90		dB
Total RMS Noise			91.6		μVRMS
Signal-to-Noise Ratio	fIN = 1 kHz	87.5	89.5		dB
	fIN = 100 kHz		88.5		dB
	fIN = 400 kHz		88		dB
	fIN = 1 MHz		87.5		dB
Signal-to-Noise + Distortion (SINAD)	fIN = 1 kHz	87.3	89		dB
	fIN = 100 kHz		88		dB
	fIN = 400 kHz		87.5		dB
	fIN = 1 MHz		87		dB
Total Harmonic Distortion (THD)	fIN = 1 kHz		-115		dB
	fIN = 100 kHz		-111		dB
	fIN = 400 kHz		-106		dB
	fIN = 1 MHz		-90		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ²
Spurious-Free Dynamic Range	$f_{IN} = 1 \text{ kHz}$		114		dB
	$f_{IN} = 100 \text{ kHz}$		110		dB
	$f_{IN} = 400 \text{ kHz}$		105		dB
	$f_{IN} = 1 \text{ MHz}$		91		dB
	–3 dB Input Bandwidth, RC Filter			42	
Aperture Delay ⁹			0		ns
Aperture Jitter ⁹			0.25		pSRMS
REFERENCE					
REFIN, Internal Reference Output Voltage	Output current (I_{OUT}) = 0 μA	2.028	2.048	2.068	V
Temperature Coefficient			± 5	± 20	ppm/ $^{\circ}\text{C}$
Output Impedance			15		k Ω
Line Regulation	VDD = 4.75 V to 5.25 V		0.3		mV/V
Input Voltage Range	REFIN overdriven	2.028	2.048	2.068	V
REFBUF, Reference Buffer Output Voltage	REFIN = 2.048 V	4.056	4.096	4.136	V
Input Voltage Range	REFBUF overdriven ¹⁰	4.056	4.096	4.136	V
Load Current	REFBUF = 4.096 V (REFBUF overdriven)		1.6	1.8	mA
			0.5		mA
VCMO ¹¹					
Common-Mode Output Voltage	REFBUF = 4.096 V, $I_{OUT} = 0 \mu\text{A}$	2.028	2.048	2.028	V
Output Impedance	$-1 \text{ mA} < I_{OUT} < +1 \text{ mA}$		15		Ω
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage, V_{IL}	VIO = 2.5 V			0.6	V
Input High Voltage, V_{IH}	VIO = 2.5 V	1.7			V
Digital Input Current	VIN = 0 V to 2.5 V	–10		+10	μA
Input Pin Capacitance			3		pF
CNV+/CNV– and CLK+/CLK– (LVDS Clock Input)					
Differential Input Voltage, V_{ID}		175	350	650	mV
Common-Mode Input Voltage, V_{ICM}		0.8	1.25	1.7	V
DCO+/DCO–, DA+/DA–, and DB+/DB– (LVDS Outputs)					
Differential Output Voltage, V_{OD}	100 Ω differential load	247	350	454	mV
Common-Mode Output Voltage, V_{OS}	100 Ω differential load	1.125	1.25	1.375	V
POWER-DOWN MODE					
ADC Driver (PDB_AMP)/ ADC (PDB_ADC)					
Low	Power-down mode		<1		V
High	Enabled, normal operation		>1.7		V
POWER REQUIREMENTS					
VDD		4.75	5	5.25	V
VS+		3	5	VS– + 10	V
VS–		VS+ – 10	0	+0.1	V
VIO		2.375	2.5	2.625	V
Total Standby Current ^{12, 13}	Static, all devices enabled		45	52	mA
	Static, all devices disabled		0.1	0.4	μA
ADAQ23875 Current Draw					
VDD			4.6	5	mA
VS+/VS–			4	5.5	mA
VIO			40	42	mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit ²
ADAQ23875 Power Dissipation	VDD = 5 V, VS+ = 5 V, VS- = 0 V				
VDD			23	26.25	mW
VS+/VS-			20	28.875	mW
VIO	One-lane mode ¹⁴		100	110.25	mW
Total			143	165.375	mW
TEMPERATURE RANGE					
Specified Performance	T _{MIN} to T _{MAX}	-40		+85	°C

¹ For gain = 2, limit the differential input range, V_{IN}, to 95% to allow enough footroom for the ADC driver with VS- = 0 V to achieve the specified performance.

² The LSB unit means least significant bit. The weight of the LSB, referred to input, changes depending on the input voltage range.

³ The differential input ranges, V_{IN}, must be within the allowed input common-mode range as per Figure 3 to Figure 7. V_{IN} is dependent on the VS+ and VS- supply rails used.

⁴ The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADAQ23875 running at a throughput rate of 15 MSPS.

⁵ f_s = 15 MHz, and the REFBUF current (I_{REFBUF}) varies linearly with throughput rate.

⁶ The transient response is the time required for the ADAQ23875 to acquire a full-scale input step to within ±1 LSB accuracy. Guaranteed by design, not subject to test.

⁷ See the 1/f noise plot in Figure 25.

⁸ All ac specifications expressed in decibels are referenced to the full-scale input range (FSR) and are tested with an input signal at 1 dB below full scale, unless otherwise specified.

⁹ Guaranteed by design, not subject to test.

¹⁰ When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN = 0 V. Refer to the Voltage Reference Input section for more information.

¹¹ The VCMO voltage can be used for other circuitry. However, drive the voltage with a buffer to ensure the VCMO voltage remains stable as per the specified range.

¹² With all digital inputs forced to VIO or GND, as required.

¹³ During the acquisition phase.

¹⁴ In two-lane mode, the VIO power dissipation is about 10 mW higher than one-lane mode.

TIMING SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS- = -1 V ± 5%, VS- = 0 V¹ (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, f_s = 15 MSPS, gain = 2, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f _{SAMPL}	0.02		15	MSPS
Conversion Time—CNV± Rising Edge to Data Available	t _{CONV}	54	58	63	ns
Acquisition Phase	t _{ACQ}		t _{CYC} - 39		ns
Time Between Conversions	t _{CYC}	66.6		50,000	ns
CNV± High Time	t _{CNVH}	5			ns
CNV± Low Time	t _{CNVL}	8			ns
CNV± Rising Edge to First CLK± Rising Edge from the Same Conversion	t _{FIRSTCLK}	65			ns
CNV± Rising Edge to First CLK± Falling Edge from the Previous Conversion	t _{LASTCLK}			49	ns
CLK± to DCO± Delay	t _{CLKDCO}	0.7	1.3	2.3	ns
CLK± Low Time	t _{CLKL}	1.25			ns
CLK± High Time	t _{CLKH}	1.25			ns
CLK± to DA± and DB± Delay	t _{CLKD}	0.7	1.3	2.3	ns
DCO± to DA± and DB± Skew ¹	t _{SKEW}	-200	0	+200	ns
Sampling Delay Time	t _{AP}		0		ns
Sampling Delay Jitter	t _{JITTER}		0.25		ns

¹ See Figure 4 (t_{SKEW} = t_{CLKD} - t_{CLKDCO}).

Timing Diagrams

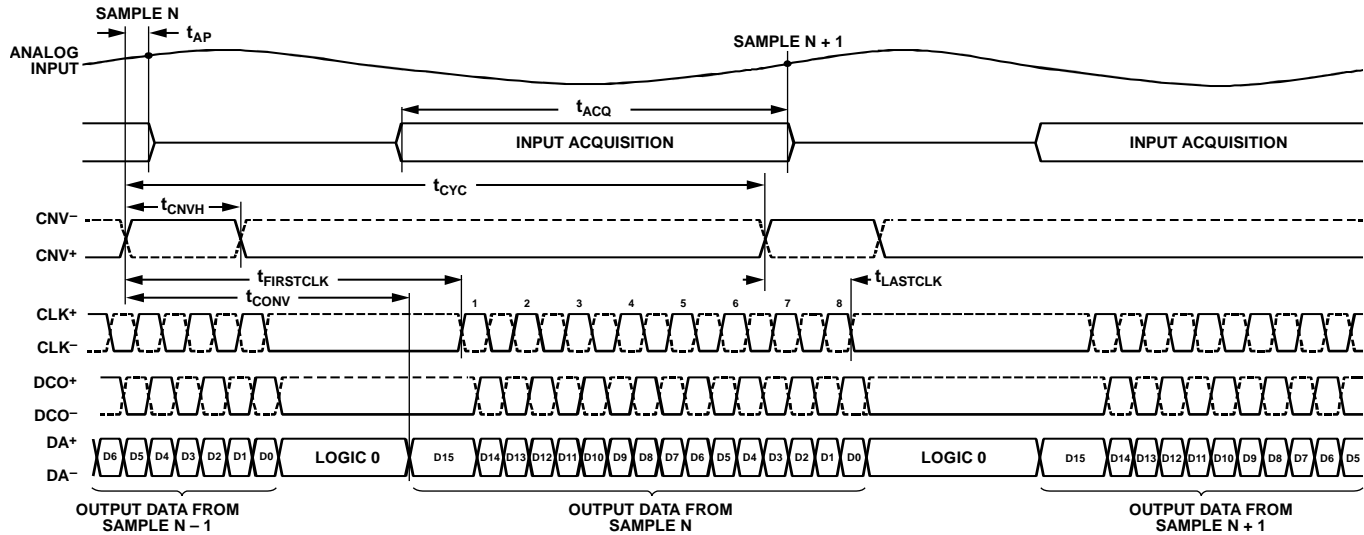


Figure 2. One-Lane Output Mode Timing Diagram

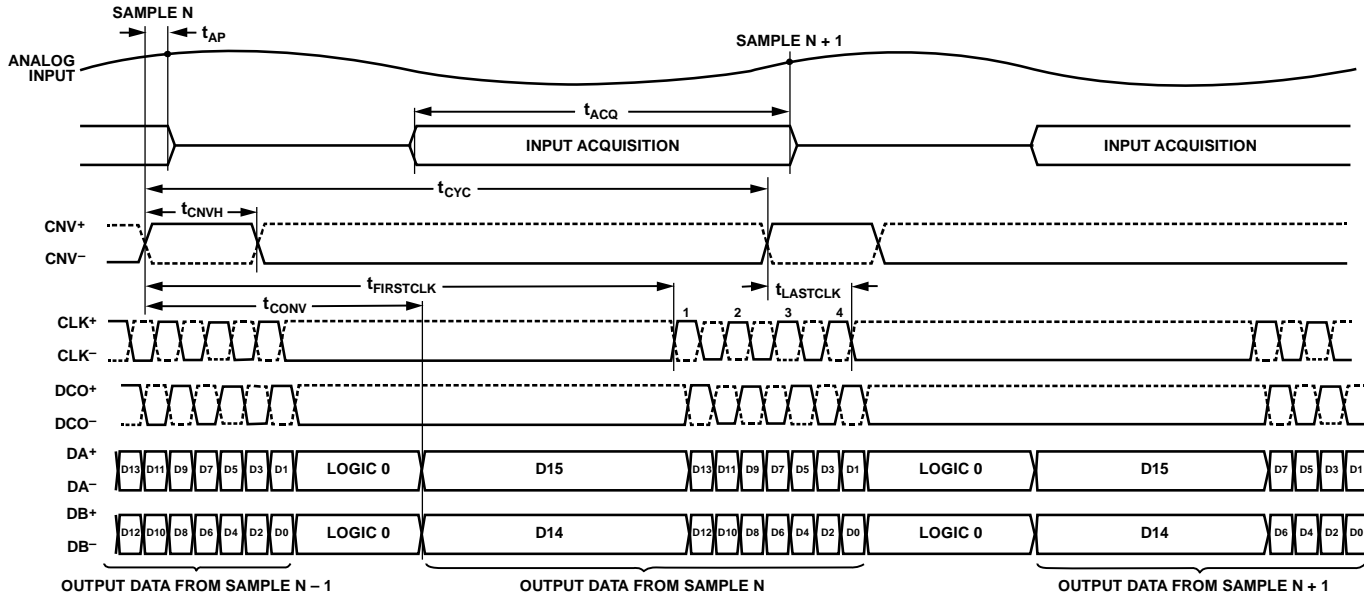


Figure 3. Two-Lane Output Mode Timing Diagram

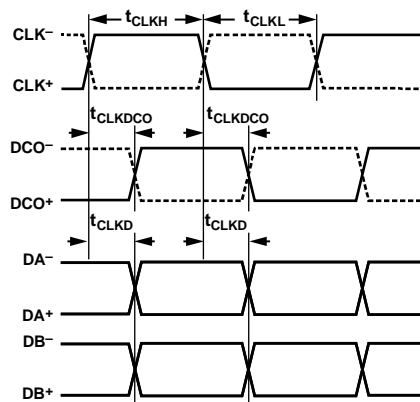


Figure 4. Data Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Inputs	
IN1+, IN1– to GND	–12 V to +12 V or ± 24 mA
Supply Voltage	
VDD to GND	6 V
VIO to GND	2.8 V
VS+ to VS–	11 V
VS+ to GND	–0.3 V to +11 V
VS– to GND	–11 V to +0.3 V
REFBUF to GND	–0.3 V to VDD + 0.3 V
REFIN to GND	–0.3 V to +2.8 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type ¹	θ_{JA}	θ_{JC}	Unit
BC-100-7	48.4	35.1	°C/W

¹ Test Condition 1: thermal impedance simulated values are based on use of a 252P JEDEC PCB.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for the handling of ESD sensitive devices in an ESD protected area only.

The human body model (HBM) is per ANSI/ESDA/JEDDEC JS-001.

The field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 5. ADAQ23875, 100-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	3000	2
FICDM	1500	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10
A	GND	IN1-	IN1+	GND	GND	GND	GND	VIO	GND	CNV+
B	PDB_AMP	IN1-	IN1+	GND	GND	GND	GND	TWOLANES	GND	CNV-
C	GND	VS+	GND	VS+	VS-	GND	GND	GND	GND	GND
D	GND	GND	GND	GND	GND	VCMO	GND	GND	GND	CLK+
E	GND	GND	GND	VS+	GND	GND	GND	GND	GND	CLK-
F	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND
G	GND	GND	GND	GND	GND	GND	GND	GND	GND	DCO+
H	VS+	GND	GND	GND	GND	GND	GND	GND	GND	DCO-
J	VS-	GND	REFBUF	REFBUF	GND	GND	GND	GND	GND	DA+
K	GND	GND	REFIN	GND	PDB_ADC	VDD	TESTPAT	DB-	DB+	DA-

23875-005

Figure 5. 100-Ball CSP_BGA Pin Configuration, Top View

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
A1, A4 to A7, A9, B4 to B7, B9, C1, C3, C6 to C10, D1 to D5, D7 to D9, E1 to E3, E5 to E8, E9, F3 to F10, G1 to G9, H2 to H9, J2, J5 to J9, K1, K2, K4	GND	P	Power Supply Ground.
A2, B2	IN1-	AI	Negative Input of the FDA Connected to a 550 Ω Resistor.
A3, B3	IN1+	AI	Positive Input of the FDA Connected to a 550 Ω Resistor.
A8	VIO	P	2.5 V Analog and Output Power Supply. The range of VIO is 2.375 V to 2.625 V. The low dropout (LDO) regulator output generating the VIO supply of the μModule must be bypassed with an at least 2.2 μF (0402, X5R) ceramic capacitor to GND.
A10	CNV+	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample and hold in hold mode and starts a conversion cycle. CNV+ can also be driven with a 2.5 V CMOS signal if CNV- is connected to GND.

Pin No.	Mnemonic	Type ¹	Description
B1	PDB_AMP	DI	Active Low. Connect the PDB_AMP pin to GND to power down the FDA. Otherwise, connect the PDB_AMP pin to VS+.
B8	TWOLANES	DI	Digital Input that Enables Two-Lane Output Mode. When TWOLANES is connected high (two-lane output mode), the ADAQ23875 outputs 2 bits at a time on DA-/DA+ and DB-/DB+. When TWOLANES is low (one-lane output mode), the ADAQ23875 outputs 1 bit at a time on DA-/DA+, and DB-/DB+ are disabled. Logic levels are determined by VIO.
B10	CNV-	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample and hold in hold mode and starts a conversion cycle. CNV+ can be also driven with a 2.5 V CMOS signal if CNV- is connected to GND.
C2, C4, E4, H1	VS+	P	FDA and Reference Buffer Positive Supply. The LDO output generating the VS+ supply of μ Module must be bypassed with an at least 2.2 μ F (0402, X5R) ceramic capacitor to GND.
C5, J1	VS-	P	FDA Negative Supply. The LDO output generating the VS- supply of μ Module must be bypassed with an at least 2.2 μ F (0402, X5R) ceramic capacitor to GND.
D6	VCMO	AO	FDA Output Common-Mode Voltage. The VCMO pin is nominally REFBUF/2.
D10	CLK+	DI	LVDS Clock Input. The CLK+ pin is an externally applied clock that serially shifts out the conversion result.
E10	CLK-	DI	LVDS Clock Input. The CLK- is an externally applied clock that serially shifts out the conversion result.
F1, F2	NC		No Connect. Remove power and ground planes under the NC pins to avoid undesired parasitic capacitance. See the PCB Layout section.
G10	DCO+	DO	LVDS Data Clock Output. The DCO+ pin is an echoed version of CLK+/CLK- that can be used to latch the data outputs.
H10	DCO-	DO	LVDS Data Clock Output. The DCO- pin is an echoed version of CLK+/CLK- that can be used to latch the data outputs.
J3, J4	REFBUF	AO	Reference Buffer Output Voltage. As a required component of a SAR architecture, a 10 μ F ceramic bypass capacitor is already laid out within the ADAQ23875 between REFBUF and GND. Therefore, adding a second, smaller capacitor in parallel with the 10 μ F capacitor may degrade performance and is not recommended.
J10	DA+	DO	Serial LVDS Data Output. In one-lane output mode, DB-/DB+ are not used, and their LVDS driver is disabled to reduce power consumption.
K3	REFIN	P	Internal Reference Output/Reference Buffer Input. The output voltage of the internal reference, nominally 2.048 V, is output on the REFIN pin. An external reference can be applied to REFIN if a more accurate reference is required. If the internal reference buffer is not used, connect REFIN to GND to power down the buffer and connect an external buffered reference to REFBUF.
K5	PDB_ADC	DI	Digital Input that Enables the Power-Down Mode. When PDB_ADC is low, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) shuts down. When PDB_ADC is high, the device operates normally. Logic levels are determined by VIO.
K6	VDD	P	5 V Analog Power Supply. The range of VDD is 4.75 V to 5.25 V. The LDO output generating the VDD supply of μ Module must be bypassed with an at least 2.2 μ F (0402, X5R) ceramic capacitor to GND.
K7	TESTPAT	DI	Digital Input that Forces the LVDS Data Outputs to be a Test Pattern. When TESTPAT is high, the digital outputs are a test pattern. When TESTPAT is low, the digital outputs are the ADAQ23875 conversion result. Logic levels are determined by VIO.
K8	DB-	DO	Serial LVDS Data Output. In one-lane output mode, DA-/DA+ are not used, and their LVDS driver is disabled to reduce power consumption.
K9	DB+	DO	Serial LVDS Data Outputs. In one-lane output mode, DA-/DA+ are not used, and their LVDS driver is disabled to reduce power consumption.
K10	DA-	DO	Serial LVDS Data Outputs. In one-lane output mode, DB-/DB+ are not used, and their LVDS driver is disabled to reduce power consumption.

¹ P is power, AI is analog input, DI is digital input, AO is analog output, DO is digital output, and NC is no connect. Remove the power and ground planes under the AI, AO, DI, and DO pins to avoid undesired parasitic capacitance and impact on performance. See the Board Layout section.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS- = -1 V ± 5%, VS- = 0 V (95% of VIN), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, fs = 15 MSPS, gain = 2, and all specifications TA = 25°C, unless otherwise noted.

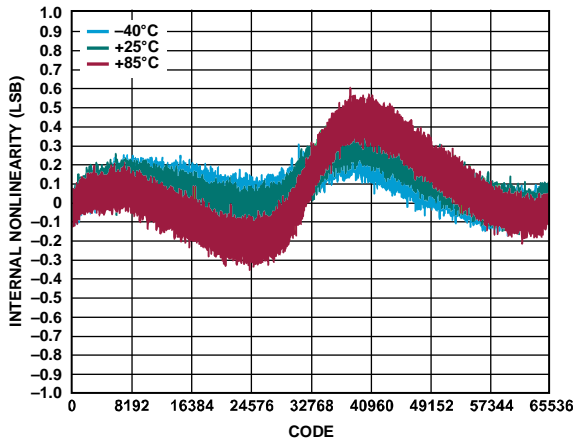


Figure 6. INL vs. Code for Various Temperatures, fs = 15 MSPS

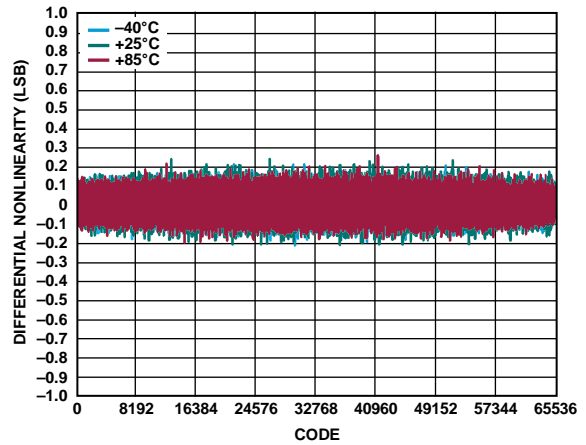


Figure 9. DNL vs. Code for Various Temperatures, fs = 15 MSPS

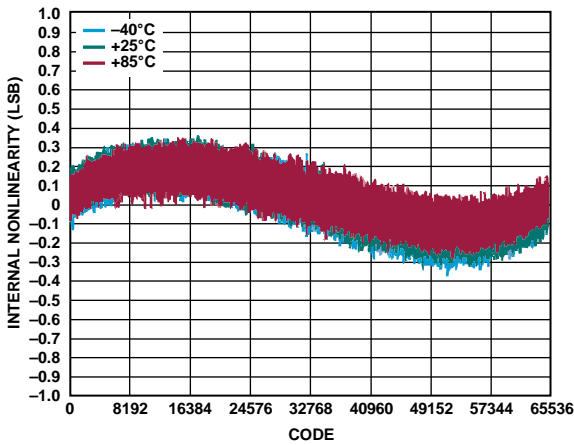


Figure 7. INL vs. Code for Various Temperatures, fs = 10 MSPS

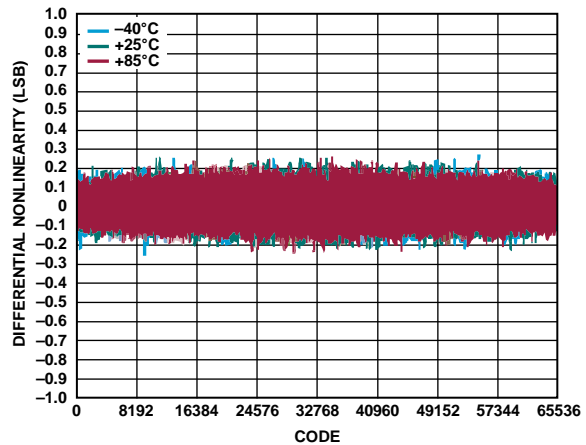


Figure 10. DNL vs. Code for Various Temperatures, fs = 10 MSPS

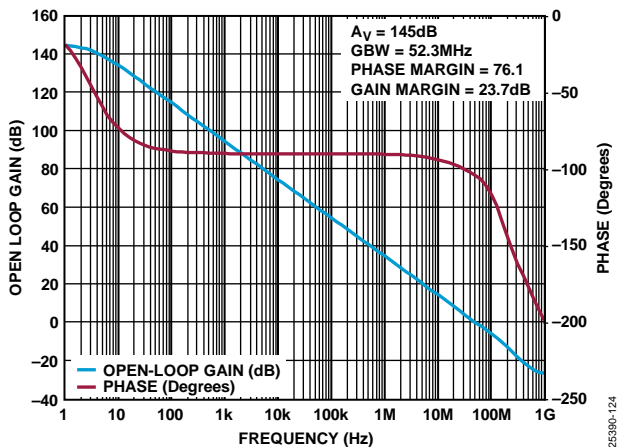


Figure 8. ADC Driver Open-Loop Gain and Phase vs. Frequency

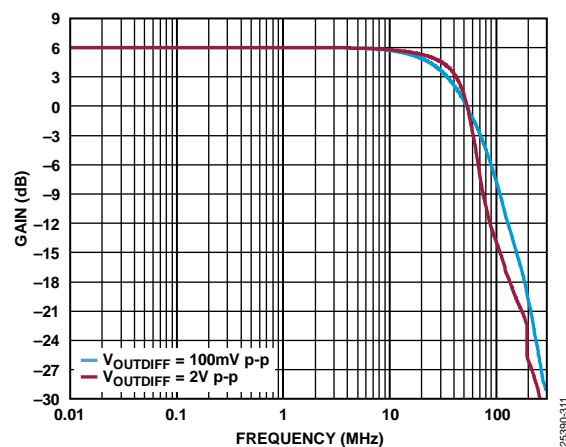


Figure 11. ADC Driver Frequency Response (VOUTDIFF Is the Differential Output Voltage)

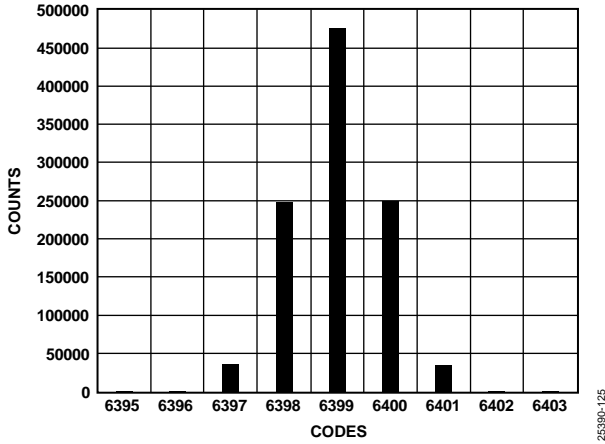


Figure 12. Histogram of a DC Input at the Code Center

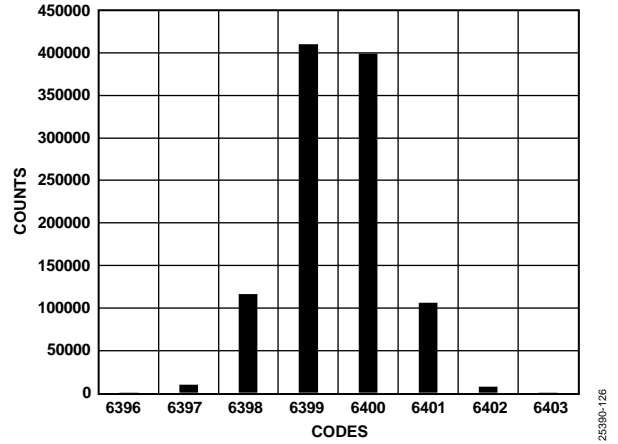


Figure 15. Histogram of a DC Input at the Code Transition

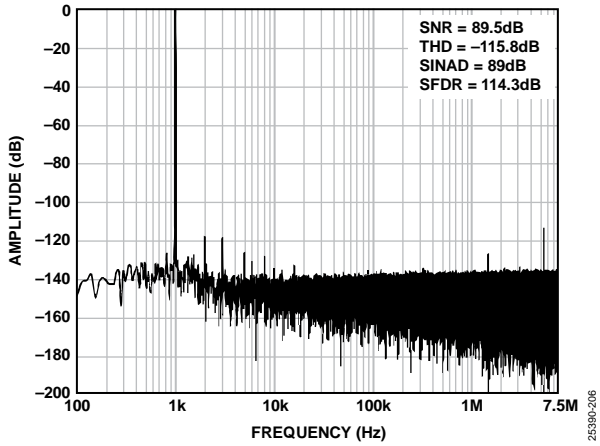


Figure 13. 1 kHz, -1 dBFS Input Tone FFT, Wide View, Differential, $f_s = 15$ MSPS

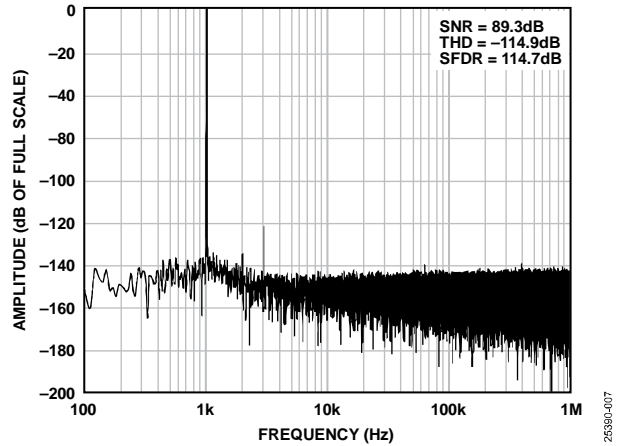


Figure 16. 1 kHz, -1 dBFS Input Tone FFT, Wide View, Differential, $f_s = 10$ MSPS

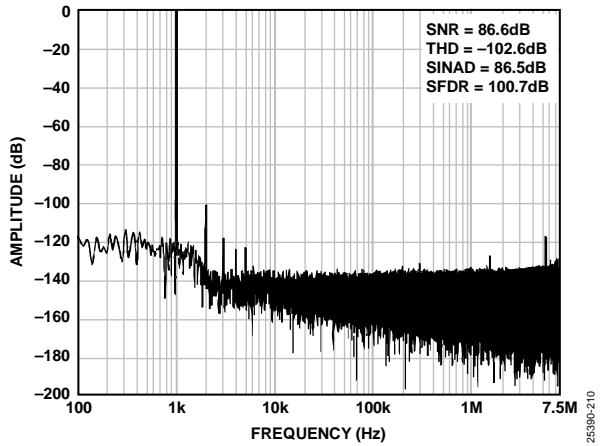


Figure 14. 1 kHz, -1 dBFS Input Tone FFT, Wide View, Single-Ended, $VC_{MO} = 0$ V

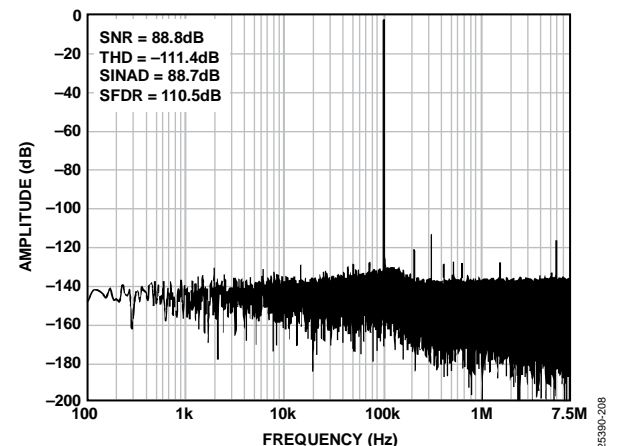


Figure 17. 100 kHz, -3 dBFS Input Tone FFT, Wide View, Differential

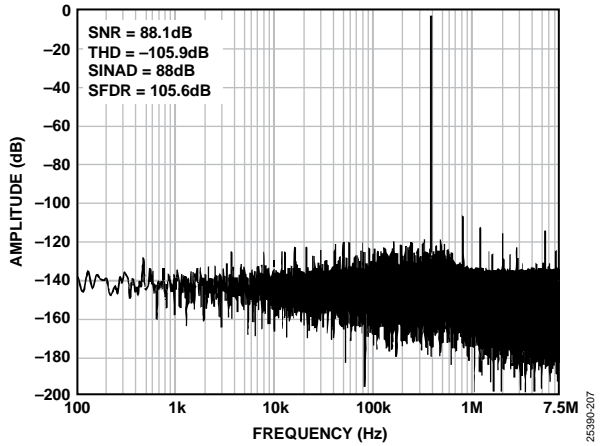


Figure 18. 400 kHz, -3 dBFS Input Tone FFT, Wide View, Differential

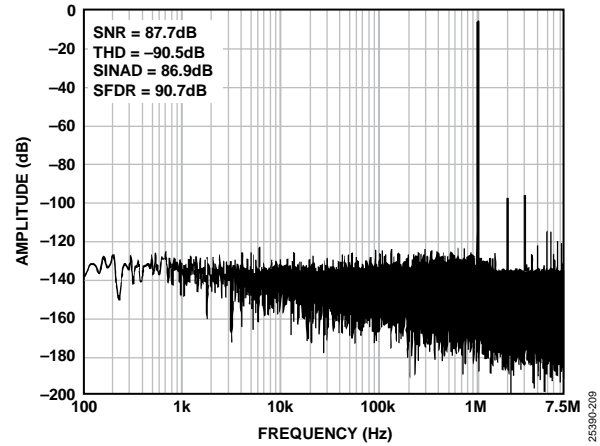


Figure 21. 1 MHz, -6 dBFS Input Tone FFT, Wide View, Differential

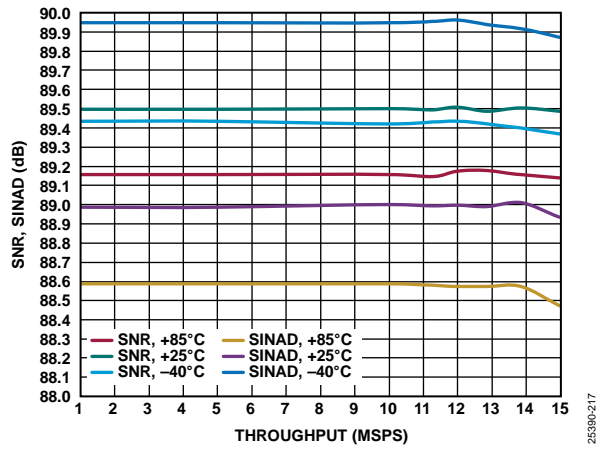


Figure 19. SNR, SINAD vs. Throughput for Various Temperatures, $f_{IN} = 1$ kHz

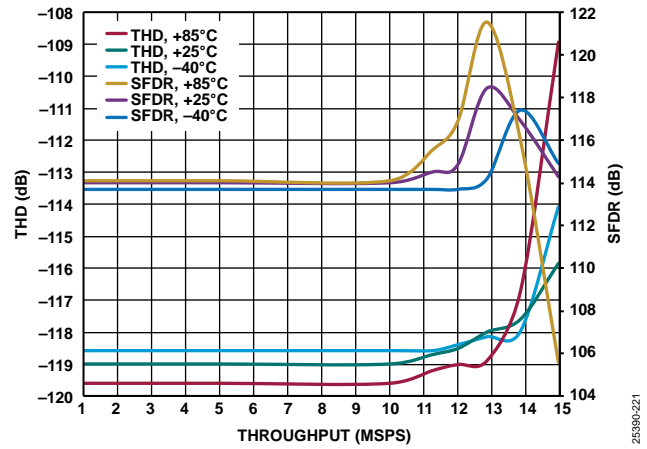


Figure 22. THD and SFDR vs. Throughput for Various Temperatures, $f_{IN} = 1$ kHz

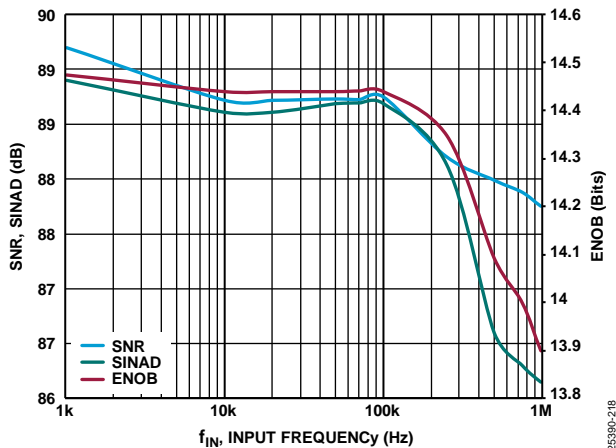


Figure 20. SNR, SINAD and ENOB vs. Input Frequency

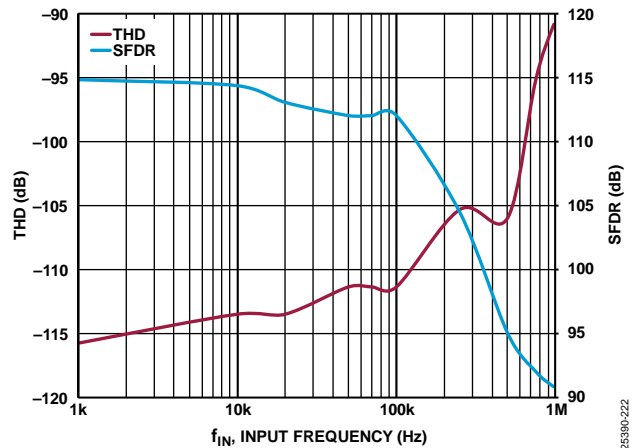


Figure 23. THD and SFDR vs. f_{IN}

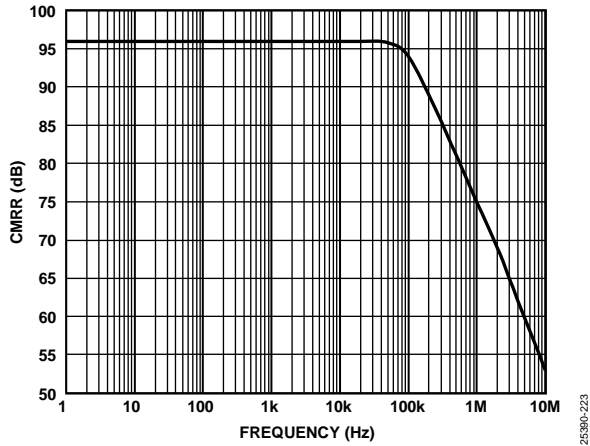


Figure 24. CMRR vs. Frequency

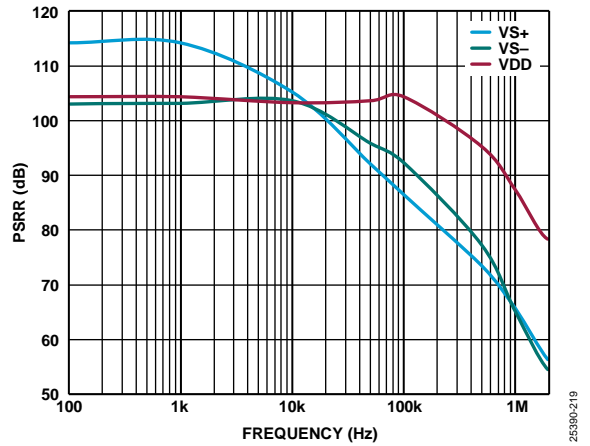


Figure 27. PSRR vs. Frequency

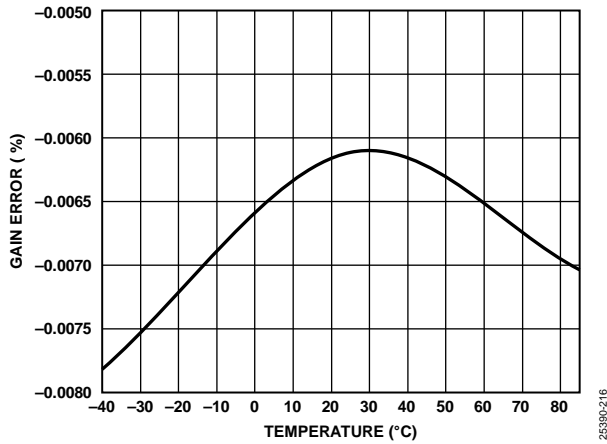


Figure 25. Gain Error vs. Temperature

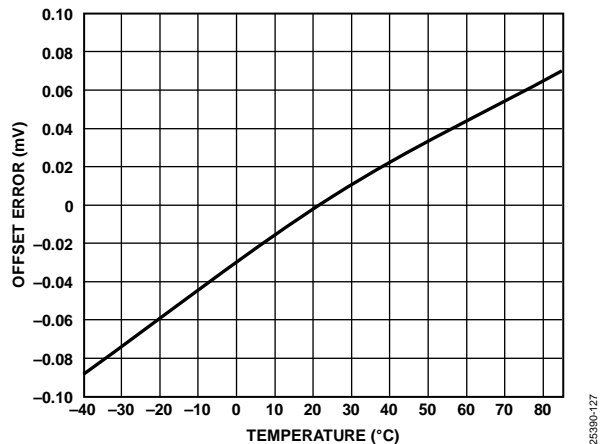


Figure 28. Offset Error vs. Temperature

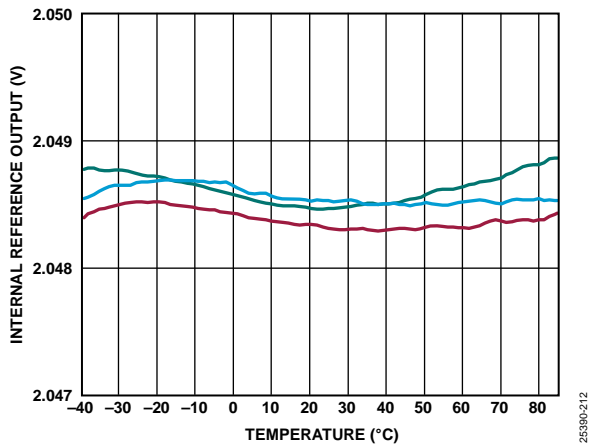


Figure 26. Internal Reference Output vs. Temperature

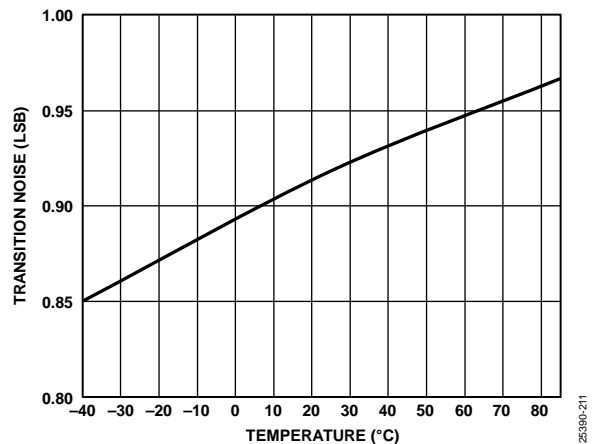


Figure 29. Transition Noise vs. Temperature

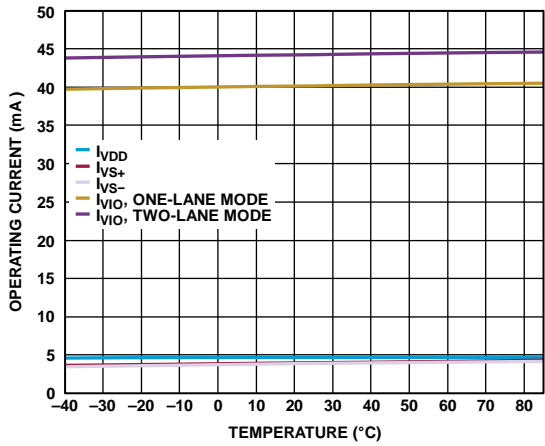


Figure 30. Operating Current vs. Temperature

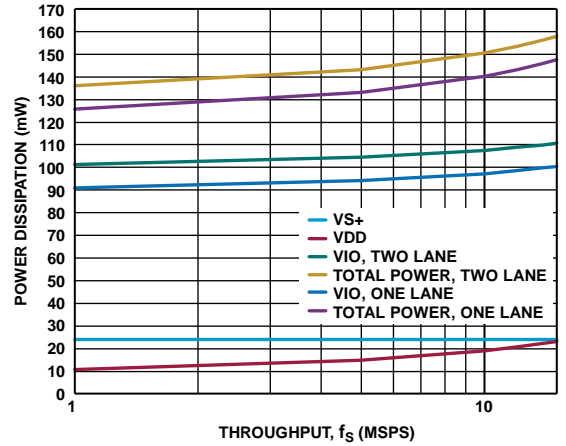


Figure 33. Power Dissipation vs. Throughput, 25°C

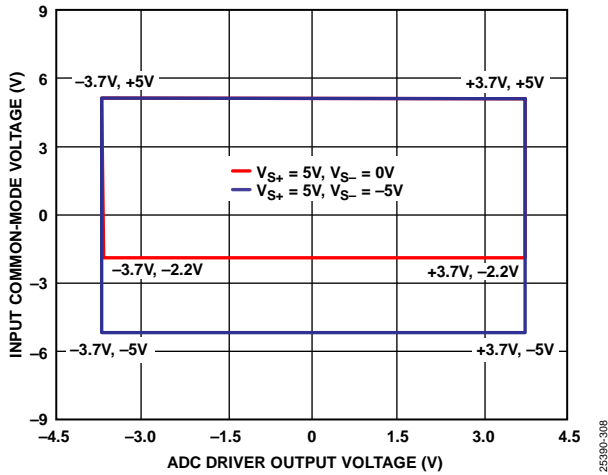


Figure 31. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 2, ±1.024 V Differential Input

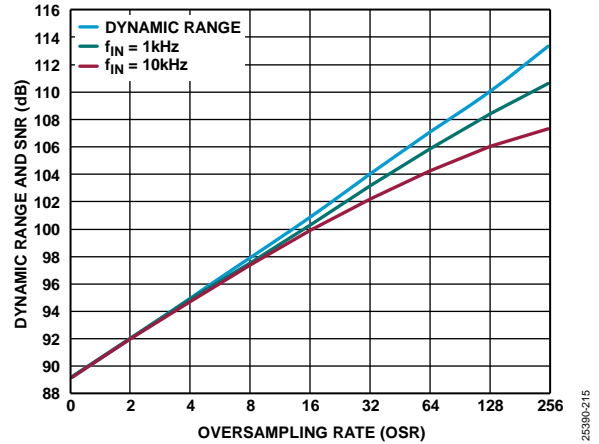


Figure 34. Dynamic Range and SNR vs. Oversampling Rate for Input Frequencies

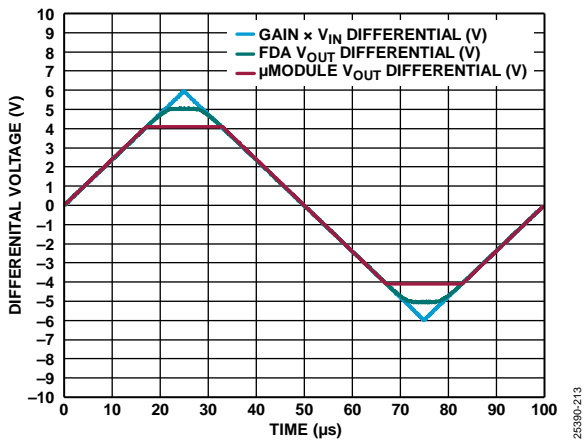


Figure 32. Output Overdrive Recovery vs. Time, $f_{IN} = 10 \text{ kHz}$

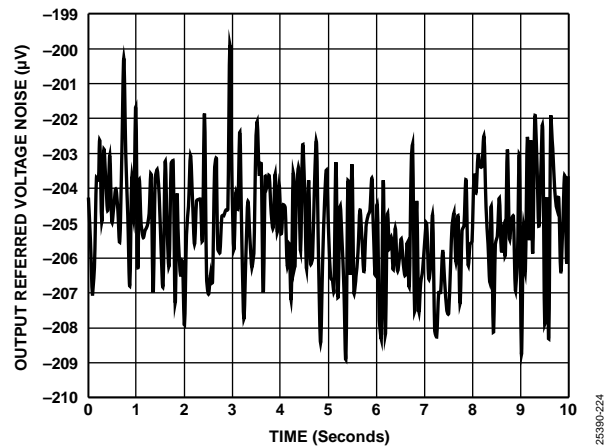


Figure 35. $1/f$ Noise for 0.1 Hz to 10 Hz Bandwidth, $f_s = 100 \text{ kSPS}$, 256 Samples Averaged per Reading, OSR = 4096

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line

Differential Nonlinearity (DNL)

In an ideal μ Module, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The first transition occurs at a level ½ LSB above analog ground (62.5 μ V for the gain = 2, ± 2.048 V range). Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift

Offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full-scale code range (gain = 2, ± 2.048 V range). This drift is expressed in parts per million per degree Celsius as follows:

$$\text{Offset Error Drift (ppm/}^\circ\text{C)} = 10^6 \times (\text{Offset Error}_{T_{MAX}} - \text{Offset Error}_{T_{MIN}}) / (T_{MAX} - T_{MIN})$$

where: $T_{MAX} = 85^\circ\text{C}$ and $T_{MIN} = -40^\circ\text{C}$.

Gain Error

The first transition (from 100 ... 000 to 100 ... 001) occurs at a level ½ LSB above nominal negative full scale (-4.0959375 V for gain = 2, ± 2.048 V range) and the last transition (from 011 ... 110 to 011 ... 111) occurs for an analog voltage 1½ LSB below the nominal full scale ($+4.0958125$ V for the gain = 2, ± 2.048 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the ideal levels after the offset error is removed. This error is expressed in percentage as follow:

$$\text{Gain_Error (\%)} = 100 \times ((\text{PFS-NFS})_{ACTUAL_CODE} - (\text{PFS-NFS})_{IDEAL_CODE}) / (\text{PFS-NFS})_{IDEAL_CODE}$$

where:

PFS is positive full scale.

NFS is negative full scale.

Gain Error Drift

Gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range (gain = 2, ± 2.048 V range). This drift is expressed in parts per million per degree Celsius as follows:

$$\text{Gain Error Drift (ppm/}^\circ\text{C)} = 10^6 \times (\text{Gain Error}_{T_{MAX}} - \text{Gain Error}_{T_{MIN}}) / (T_{MAX} - T_{MIN})$$

where: $T_{MAX} = 85^\circ\text{C}$ and $T_{MIN} = -40^\circ\text{C}$.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD and expressed in bits as follows:

$$\text{ENOB (bits)} = (\text{SINAD}_{dB} - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. This range is measured with a signal at -60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the μ Module to acquire a full-scale input step to ± 1 LSB accuracy.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the μ Module output at the frequency, f , to the power of a 1.3 V p-p sine wave applied to the input common-mode voltage of frequency, f .

$$\text{CMRR (dB)} = 10 \log(P_{\mu\text{Module_IN}} / P_{\mu\text{Module_OUT}})$$

where:

$P_{\mu\text{Module_IN}}$ is the common-mode power at the frequency, f , applied to the inputs.

$P_{\mu\text{Module_OUT}}$ is the power at the frequency, f , in the μ Module output.

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the μ Module output at the frequency, f , to the power of a 500 mV p-p sine wave applied to the VDD and VS+ supply voltage centered at 5 V and 100 mV p-p for a VS- supply voltage centered at -1 V of frequency, f .

$$PSRR \text{ (dB)} = 10 \log(P_{\mu\text{Module_IN}}/P_{\mu\text{Module_OUT}})$$

where:

$P_{\mu\text{Module_IN}}$ is the power at the frequency, f , at each of the VDD, VS+ and VS- supply pins.

$P_{\mu\text{Module_OUT}}$ is the power at the frequency, f , in the μ Module output.

THEORY OF OPERATION

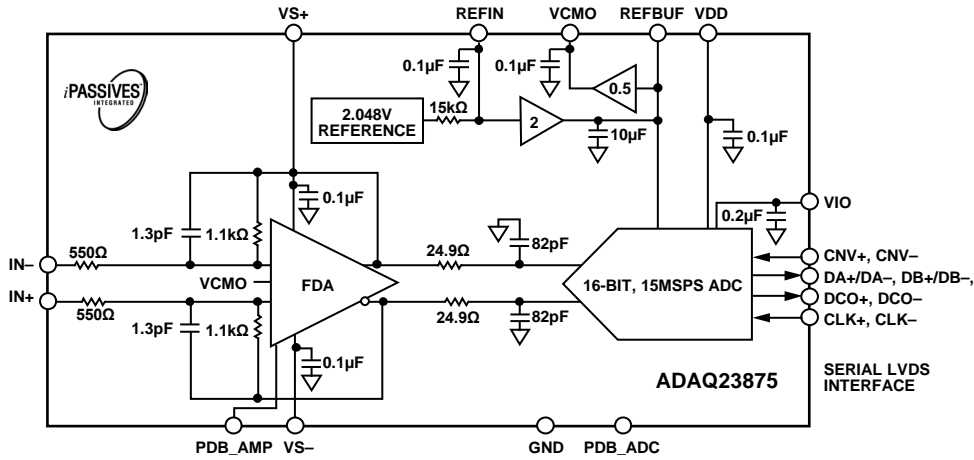


Figure 36. ADAQ23875 μModule Simplified Block Diagram

CIRCUIT INFORMATION

The ADAQ23875 is a precision, high speed, μModule data acquisition solution that reduces the development cycle of precision measurement systems by transferring the design burden of component selection, optimization, and layout from the designer to the device. The ADAQ23875 reduces the end system component count by combining multiple common signal processing and conditioning blocks in a single device, including a low noise, FDA, a stable reference buffer, and a high speed, 16-bit, 15 MSPS, SAR ADC. The device also incorporates the Analog Devices proprietary iPassive technology components necessary for optimum performance. The superior matching and drift characteristics of the resistors minimizes temperature dependent error sources.

The ADAQ23875 includes a precision internal 2.048 V reference, as well as an internal reference buffer. The ADAQ23875 also has a high speed serial LVDS interface that can output one or two bits at a time. The fast 15 MSPS throughput with no pipeline latency makes the ADAQ23875 ideally suited for a wide variety of high speed applications. The ADAQ23875 typically dissipates only 143 mW at 15 MSPS. The ADAQ23875 output is always valid because the FDA outputs fully recover within the full-scale range (± 4.096 V) of the ADC, as shown in Figure 31.

TRANSFER FUNCTION

The ADAQ23875 μModule digitizes the full-scale voltage of $2 \times \text{REFBUF}$ in to 2^{16} levels, resulting in an LSB size of $125 \mu\text{V}$ with $\text{REFBUF} = 4.096$ V. The output data is in twos complement format. The ideal transfer function is shown in Figure 37. The ideal offset binary transfer function can be obtained from the twos complement transfer function by inverting the MSB of each output code.

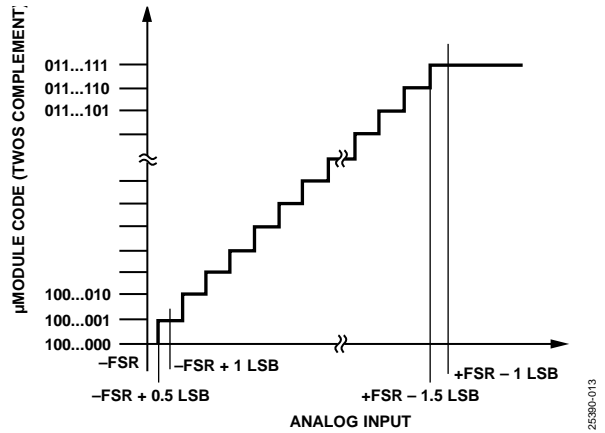


Figure 37. ADAQ23875 Ideal Transfer Function (FSR Is Full-Scale Range)

Table 7. Output Codes and Ideal Input Voltages

Description	Inputs Voltages	Digital Output Code (Twos Complement, Hex.)
FSR - 1 LSB	$(32,767 \times V_{\text{REF}}) / (32,768 \times \text{gain})$	0x7FFF
Midscale + 1 LSB	$V_{\text{REF}} / (32,768 \times \text{gain})$	0x0001
Midscale	0 V	0x0000
Midscale - 1 LSB	$-V_{\text{REF}} / (32,768 \times \text{gain})$	0xFFFF
-FSR + 1 LSB	$-(32,767 \times V_{\text{REF}}) / (32,768 \times \text{gain})$	0x8001
-FSR	$-V_{\text{REF}} \times \text{gain}$	0x8000

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAM

Figure 38 shows the typical application examples of differential signals applied to each of the ADAQ23875 inputs for a given gain with varying common-mode voltages. Figure 39 shows the

typical application example of a single-ended signal applied to one of the ADAQ23875 inputs for a given gain with a fixed common-mode voltage of 0 V.

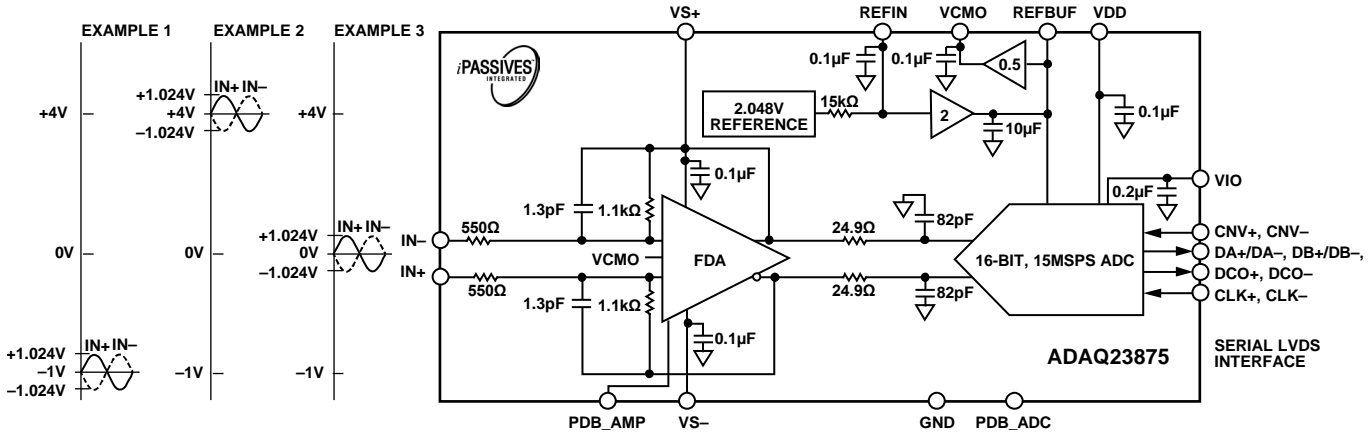


Figure 38. ADAQ23875 Differential Input Configuration with Gain = 2, ±2.048 V Input Range

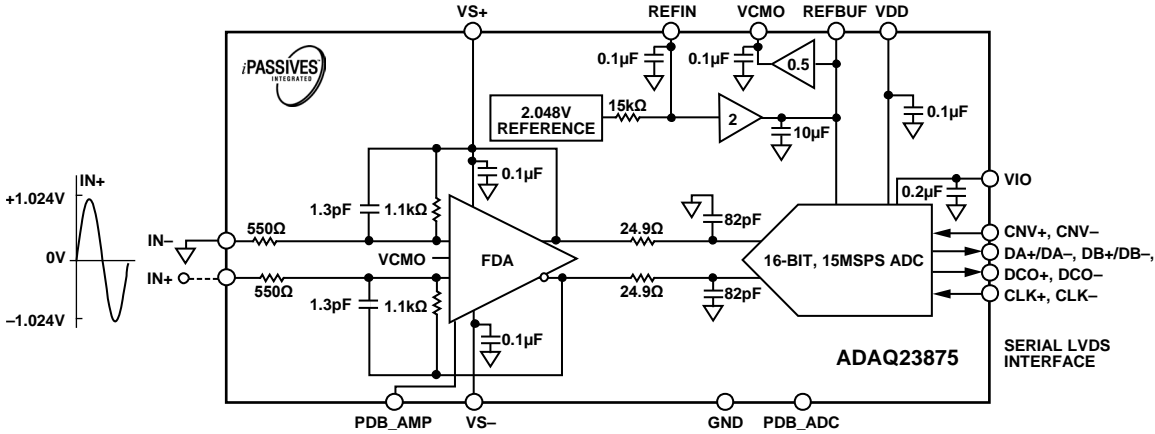


Figure 39. ADAQ23875 Single-Ended Input Configuration with Gain = 2, ±2.048 V Input Range

VOLTAGE REFERENCE INPUT

The ADAQ23875 μ Module has an internal low noise, low drift (20 ppm/ $^{\circ}$ C), band gap reference connected to REFIN. An internal reference buffer gains the REFIN voltage by $2\times$ to 4.096 V at the REFBUF pin. The voltage difference between REFBUF and GND determines the full-scale input range of the ADAQ23875. The reference and reference buffer can also be externally driven if desired. In addition, housed in the ADAQ23875 is a 10 μ F decoupling capacitor between REFBUF and GND that is ideally laid out within the device. This decoupling capacitor is a required component of the SAR architecture. Adding a second, smaller capacitor in parallel with the 10 μ F capacitor may degrade performance and is not recommended.

Internal Reference with Internal Reference Buffer

To use the internal reference and internal reference buffer, bypass the REFIN pin to GND with a 0.1 μ F ceramic capacitor.

External Reference with Internal Reference Buffer

If more accuracy and/or lower drift is required, REFIN can be directly overdriven by an external 2.048 V reference as shown in Figure 40. Analog Devices offers a portfolio of high performance references designed to meet the needs of many applications. With small size, low power, and high accuracy, the LTC6655 is well suited for use with the ADAQ23875 when overdriving the internal reference. The LTC6655 offers 0.025% (maximum) initial accuracy and 2 ppm/ $^{\circ}$ C (maximum) temperature coefficient for high precision applications.

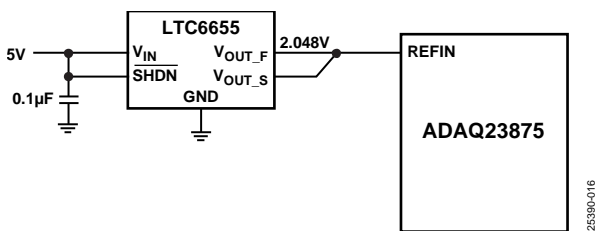


Figure 40. Using the LTC6655 as an External Reference

External Reference Buffer

The internal reference buffer can also be overdriven with an external 4.096 V reference at REFBUF as shown in Figure 41. To do so, REFIN must be grounded to disable the reference buffer. The external reference must have a fast transient response and be able to drive the 0.5 mA to 1.6 mA load at the REFBUF pin. The LTC6655 is recommended when overdriving REFBUF.

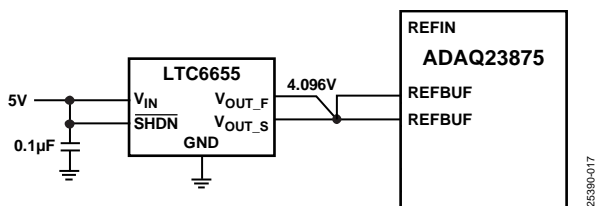


Figure 41. Overdriving REFBUF Using the LTC6655

COMMON-MODE OUTPUT

The VCMO pin is an output that nominally provides one half the voltage present on the REFBUF pin. This voltage is used to set the common mode of an FDA driving the analog inputs of the ADC in the ADAQ23875.

POWER SUPPLY

The ADAQ23875 uses four power supplies: an internal ADC core supply (VDD), a digital input/output interface supply (VIO), an FDA positive supply (VS+), and a negative supply (VS-). Figure 33 shows the typical total power dissipation including individual consumption for each of the VS+, VDD, and VIO supplies. Figure 27 shows the ADAQ23875 PSRR performance for various frequencies and the ability of the μ Module to reject any supply noise and reduce sensitivity to perturbations. Good quality ceramic bypass capacitors of at least 2.2 μ F (0402, X5R) must be placed at the output of LDO regulators generating the μ Module supply rails (VDD, VIO, VS+, and VS-) to minimize electromagnetic interference (EMI) susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ23875, improving overall subsystem PSRR and saving extra board space and cost.

See the PCB Layout section for the layout guidelines.

Power Supply Sequencing

The ADAQ23875 does not have any specific power supply sequencing requirements. The internal ADC core of ADAQ23875 has a power-on-reset (POR) circuit that resets the ADAQ23875 at initial power-up or whenever VDD drops well below the minimum values. After the supply voltage re-enters the nominal supply voltage range, the POR reinitializes the ADAQ23875.

Power-Down Mode

The power-down mode of the FDA is asserted by applying a low logic level (GND) to the PDB_AMP pin to minimize the quiescent current consumed when the ADAQ23875 is not used. When the PDB_AMP pin is connected to GND, the FDA output is high impedance. When PDB_ADC is low logic level, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) shuts down. When PDB_AMP and PDB_ADC are connected to a high logic level, the ADAQ23875 operates normally. The logic levels for both the PDB_AMP and PDB_ADC pins are determined by VS+ and VIO, respectively.

DIGITAL INTERFACE

The ADAQ23875 conversion is controlled by the CNV+ and CNV- inputs, which can be driven directly with an LVDS signal. Alternatively, the CNV+ pin can be driven with a 0 V to 2.5 V CMOS signal when CNV- is connected to GND. A rising edge on CNV+ samples the analog inputs and initiates a conversion. The pulse width of CNV+ must meet the t_{CNVH} and t_{CNVL} specifications detailed in the timing table (see Table 2).

After the ADAQ23875 is powered on or exits power-down mode, conversion data is invalid for the first two conversion cycles. The subsequent conversion results are accurate as long as the time between conversions meets the t_{CYC} specification. If the analog input signal has not completely settled when it is sampled, the ADAQ23875 noise performance is affected by jitter on the rising edge of CNV+. In this case, drive the rising edge of CNV+ with a clean, low jitter signal. Note that the ADAQ23875 is less sensitive to jitter on the falling edge of CNV+. In applications that are insensitive to jitter, CNV can be driven directly from a field programmable gate array (FPGA).

The ADAQ23875 has an internal clock that is trimmed to achieve a maximum conversion time of 63 ns. With a typical acquisition time of 27.7 ns, throughput performance of 15 MSPS is achieved.

The ADAQ23875 has a serial LVDS digital interface that is easy to connect to an FPGA. Three LVDS pairs are required: CLK±, DCO±, and DA±. A fourth LVDS pair, DB±, is optional (see Figure 42). Route the LVDS signals on the PCB as 100 Ω differential transmission lines and terminate at the receiver with 100 Ω resistors. The optional LVDS output, DB±, is enabled, and data is output 2 bits at a time on DA± and DB±. Enabling the DB± output increases the supply current from VIO by approximately 3.6 mA. In two-lane mode, four clock pulses are required for CLK± (see Figure 46).

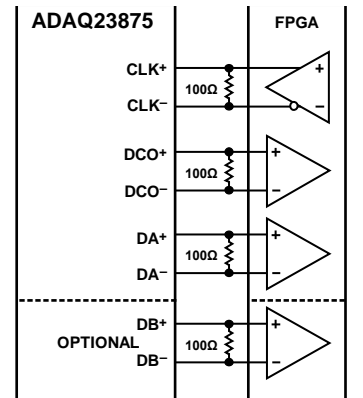


Figure 42. Digital Output Interface to an FPGA

One-Lane Output Mode

A conversion is started by the rising edge of CNV+. When the conversion is complete, the most significant data bit is output on DA±. Data is then ready to be shifted out by applying a burst of eight clock pulses to the CLK± input. The data on DA± is updated by every edge of CLK±. An echoed version of CLK± is output on DCO±. The edges of DA± and DCO± are aligned. Therefore, DCO± can be used to latch DA± in the FPGA. The timing of a single conversion is shown in Figure 43 and Figure 44. Data must be clocked out after the current conversion is complete, and before the next conversion finishes. The valid time window for clocking out data is shown in Figure 45. Note that it is allowed to still clock out data when the next conversion begins.

Two-Lane Output Mode

At high sample rates, the required LVDS interface data rate can reach >400 Mbps. Most FPGAs can support this rate, but if a lower data rate is required, the two-lane output mode can be used. When the TWOLANES input pin is connected high (VIO), the ADAQ23875 outputs 2 bits at a time on DA-/DA+ and DB-/DB+, as shown in Figure 46.

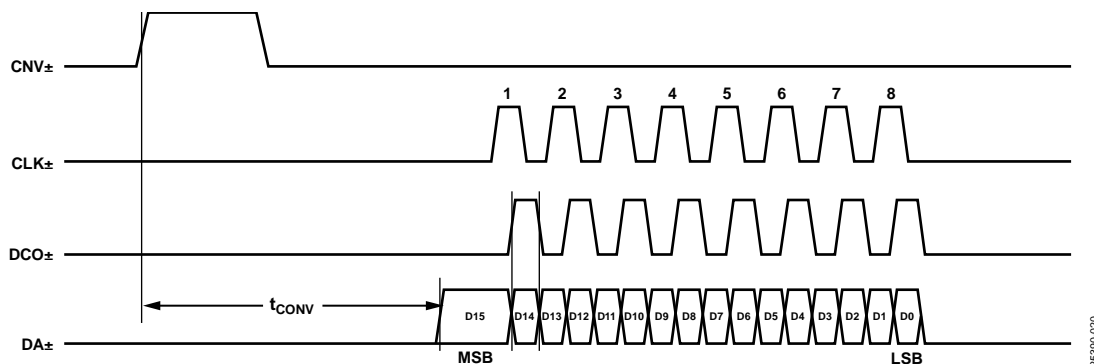


Figure 43. Timing Diagram for a Single Conversion in One-Lane Mode

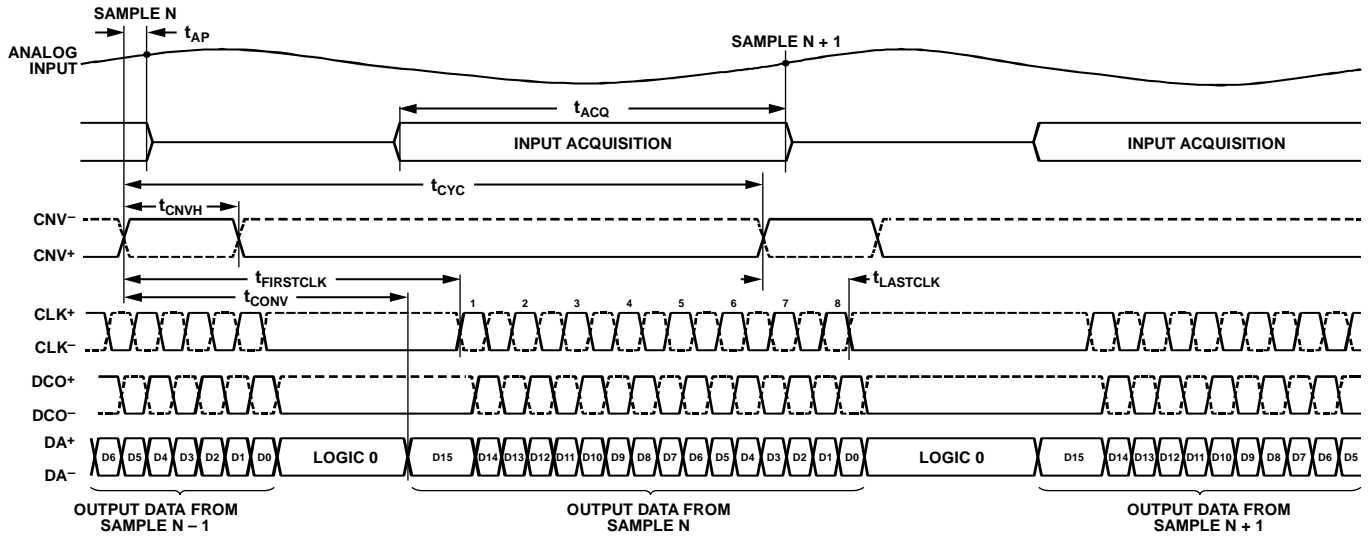


Figure 44. Timing Diagram for Multiple Conversions in One-Lane Output Mode

25390-021

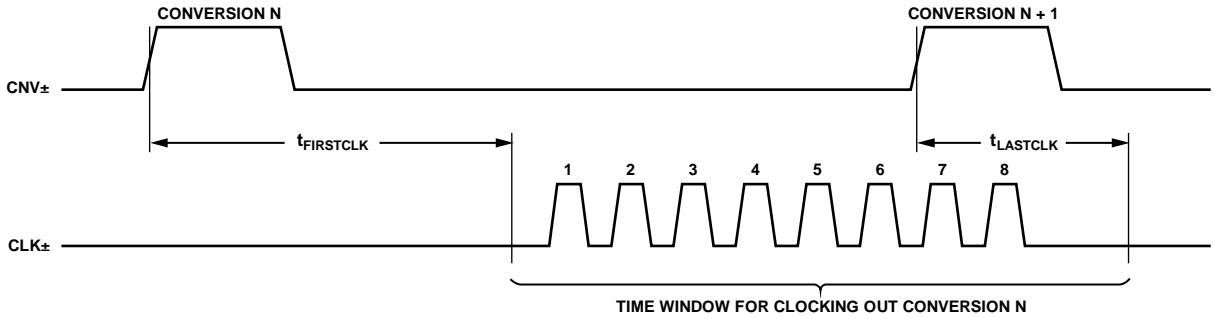


Figure 45. Valid Time Window for Clocking Out Data

25390-022

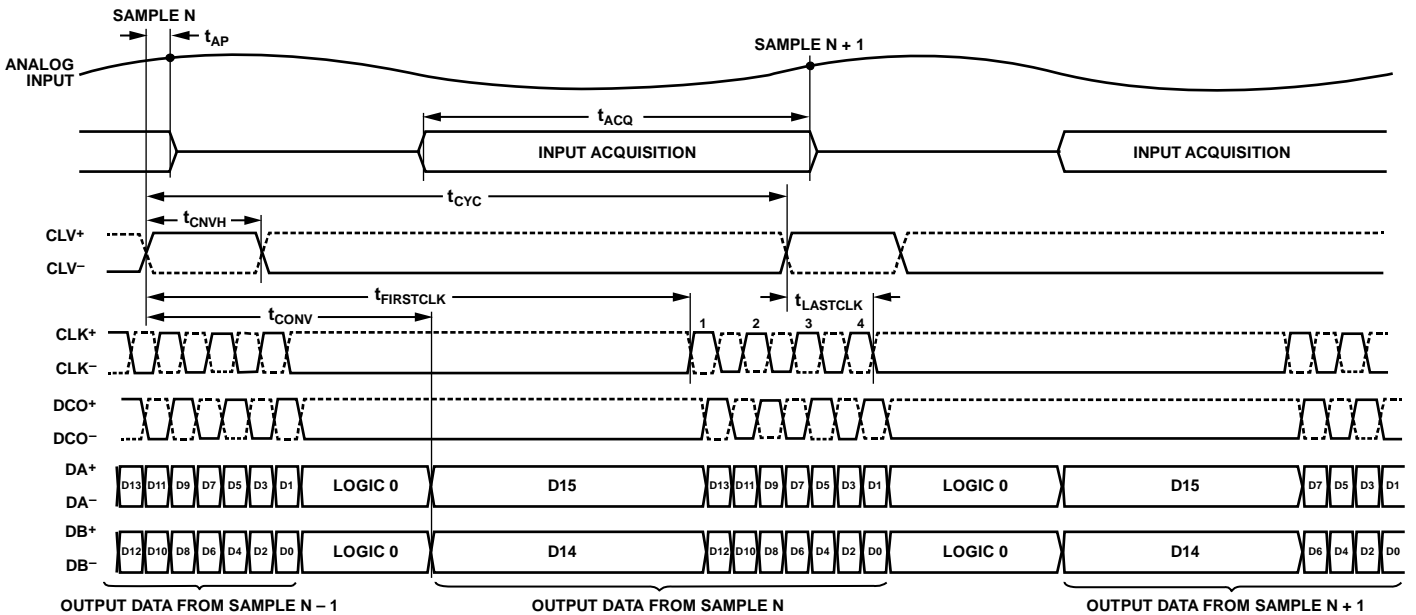


Figure 46. Two-Lane Output Mode

25390-023

Output Test Patterns

The test pattern is enabled when the TESTPAT pin is brought high (VIO) to allow in-circuit testing of the digital interface of the ADAQ23875 and forces the LVDS data outputs to be a test pattern. The ADAQ23875 digital data outputs known values as a test pattern as follows:

- One-lane mode: 1010 0000 0111 1111
- Two-lane mode: 1100 1100 0011 1111

When the TESTPAT pin is connected low (GND), the ADAQ23875 digital data outputs the conversion results.

PCB LAYOUT

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ23875. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ23875 is recommended. Care must be taken with the placement of individual components and routing of various signals on the PCB. It is highly recommended to route input and output signals symmetrically. Solder the ground pins of the ADAQ23875 directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes under the analog input/output and digital input/output (including F1 and F2) pins of ADAQ23875 to avoid undesired parasitic capacitance. Any undesired parasitic capacitance could impact the distortion and linearity performance of the ADAQ23875.

The pinout of the ADAQ23875 eases the layout, allowing its analog signals on the left side and its digital signals on the right side. The sensitive analog and digital sections must be separated on the PCB while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV_{\pm} or CLK_{\pm} , and digital outputs, DA_{\pm} and DB_{\pm} , must not run near or cross over analog signal paths to prevent noise coupling to the ADAQ23875.

Good quality ceramic bypass capacitors of at least 2.2 μF (0402, X5R) must be placed at the output of the LDO regulators generating the μ Module supply rails (VDD, VIO, VS+, and VS-) to GND to minimize EMI susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ23875, saving extra board space and cost.

Figure 47 shows the FFT sampling of the ADAQ23875 at 15 MSPS with the inputs shorted when the external decoupling capacitors on the REFIN, VDD, and VIO pins near the μ Module are removed and how well μ Module rejects any supply noise and reduces sensitivity to perturbations. This performance impact was verified on the [EVAL-ADAQ23875FMCZ](#), and no spurs are present in the noise floor, regardless of whether these external decoupling capacitors are used or removed. The recommended PCB layout is described in the [EVAL-ADAQ23875FMCZ](#) user guide.

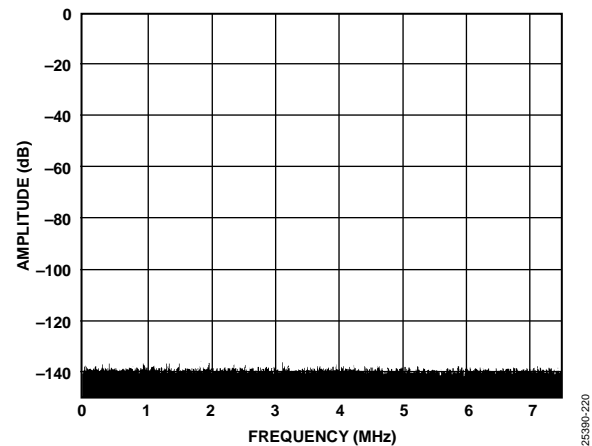


Figure 47. FFT with Shorted Inputs

Mechanical Stress Shift

The mechanical stress of mounting a device to a board may cause subtle changes to the SNR and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended.

OUTLINE DIMENSIONS

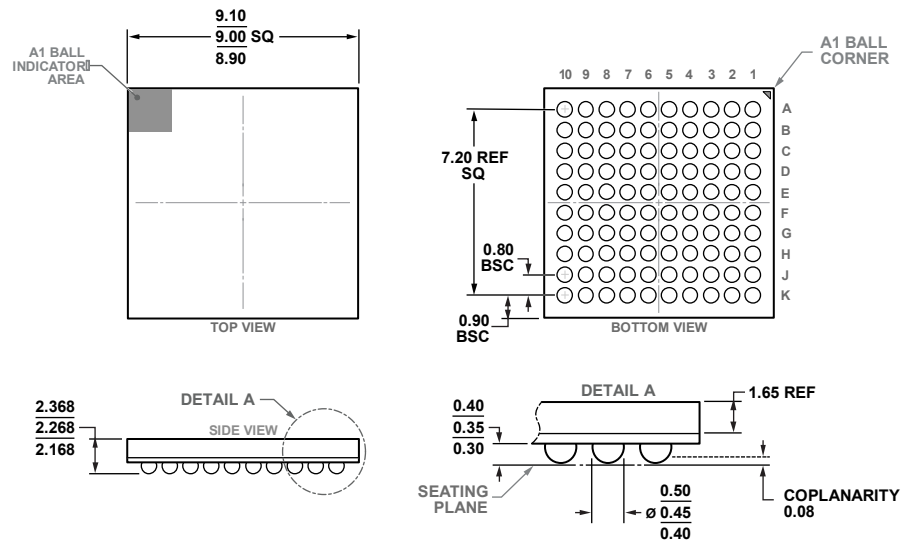


Figure 48. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADAQ23875BBCZ	-40°C to +85°C	100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-100-7
EVAL-ADAQ23875FMCZ		Evaluation Board	

¹ Z = RoHS Compliant Part.

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