



FEATURES

- Low offset voltage: 5 μ V maximum at 5.0 V and 30 V**
- Extremely low offset voltage drift: 22 nV/ $^{\circ}$ C maximum at 30 V**
- Low voltage noise density: 5.8 nV/ $\sqrt{\text{Hz}}$ typical**
- Low peak-to-peak voltage noise: 117 nV p-p from 0.1 Hz to 10 Hz typical**
- Low input bias current: 50 pA typical**
- Unity-gain crossover: 3 MHz**
- Single-supply operation: input voltage range includes ground and rail-to-rail output**
- Wide range of operating voltages**
 - Single-supply operation: 4.5 V to 55 V**
 - Dual-supply operation: ± 2.25 V to ± 27.5 V**
- Integrated EMI filters**
- Unity-gain stable**

APPLICATIONS

- Inductance, capacitance, and resistance (LCR) meter/megohmmeter front-end amplifiers**
- Load cell and bridge transducers**
- Magnetic force balance scales**
- High precision shunt current sensing**
- Thermocouple/resistance temperature detector (RTD) sensors**
- Programmable logic controller (PLC) input and output amplifiers**

GENERAL DESCRIPTION

The ADA4522-2-KGD is a dual channel, zero drift op amp with low noise and power, ground sensing inputs, and rail-to-rail output, optimized for total accuracy over time, temperature, and voltage conditions. The wide operating voltage and temperature ranges, as well as the high open-loop gain and low dc and ac errors make the device well suited for amplifying small input signals and for accurately reproducing larger signals in a wide variety of applications.

The ADA4522-2-KGD performance is specified at 5.0 V, 30 V, and 55 V power supply voltages, and the device operates over the 4.5 V to 55 V range. The ADA4522-2-KGD is an excellent selection for applications using single-ended supplies of 5 V and 30 V or for applications using higher single supplies and dual supplies of ± 2.5 V and ± 15 V. The ADA4522-2-KGD uses on-chip filtering to achieve high immunity to electromagnetic interference (EMI).

The ADA4522-2-KGD is fully specified over the -40°C to $+125^{\circ}\text{C}$ extended industrial temperature range.

Additional application and technical information can be found in the [ADA4522-2](#) data sheet.

Known Good Die (KGD): these die are fully guaranteed to data sheet specifications.

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REVISION HISTORY

10/2019—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5.0 V OPERATION

Supply voltage (V_{SY}) = 5.0 V, common-mode voltage (V_{CM}) = $V_{SY}/2$ V, and T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.7	5	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.5	15	$\text{nV}/^{\circ}\text{C}$
Input Bias Current	I_B	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		50	150	pA
Input Offset Current	I_{OS}	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		80	250	pA
Input Voltage Range	IVR		0		3.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 3.5\text{ V}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	135	155		dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 10 k Ω , output voltage (V_{OUT}) = 0.5 V to 4.5 V $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	125	145		dB
Input Resistance						
Differential Mode	R_{INDM}			30		k Ω
Common Mode	R_{INCM}			100		G Ω
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	4.97	4.98		V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	4.95		20	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}	$T_A = 125^{\circ}\text{C}$		22	30	mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^{\circ}\text{C}$		15	50	mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, closed-loop gain (A_V) = +1		4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	For single-supply operation, $V_{SY} = +4.5\text{ V to } +55\text{ V}$, and for dual-supply operation, $V_{SY} = \pm 2.25\text{ V to } \pm 27.5\text{ V}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	150	160		dB
Supply Current per Amplifier	I_{SY}	Output current (I_{OUT}) = 0 mA $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	145	830	900	μA
					950	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		1.4		V/ μ s
	SR-	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		1.3		V/ μ s
Gain Bandwidth Product	GBP	Input voltage (V_{IN}) = 10 mV p-p, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}, A_{VO} = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_{VO} = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	f_{-3dB}	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_{VO} = 1$		64		Degrees
Settling Time to 0.1%	t_s	$V_{IN} = 1\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		4		μ s
Channel Separation	CS	$V_{IN} = 1\text{ V p-p}, f = 10\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 400\text{ MHz}$		72		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 900\text{ MHz}$		80		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 1800\text{ MHz}$		83		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 2400\text{ MHz}$		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	$A_V = +1, \text{ frequency} = 1\text{ kHz}, V_{IN} = 0.6\text{ V rms}$		0.001		%
			Bandwidth = 80 kHz			
				0.02		%
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100, \text{ frequency} = 0.1\text{ Hz to }10\text{ Hz}$		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100, \text{ frequency} = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100, \text{ frequency} = 0.1\text{ Hz to }10\text{ Hz}$		16		pA p-p
Current Noise Density	i_N	$A_V = 100, \text{ frequency} = 1\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—30 V OPERATION

$V_{SY} = 30\text{ V}, V_{CM} = V_{SY}/2\text{ V}$, and $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit	
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	μ V	
					7.2	μ V	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4	22	nV/ $^\circ\text{C}$	
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	150	pA	
						500	pA
						3	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80	300	pA	
						400	pA
						500	pA
Input Voltage Range	IVR		0		28.5	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }28.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		145	160	dB	
				140		dB	
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega, V_{OUT} = 0.5\text{ V to }29.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		140	150	dB	
				135		dB	
Input Resistance	R_{INDM}			30		k Ω	
			R_{INCM}		400		G Ω
Input Capacitance	C_{INDM}			7		pF	
			C_{INCM}		35		pF

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	29.87 29.80	29.89		V V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$ to $V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		110	130 200	mV mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14		mA
Short-Circuit Current Source	I_{SC+}	$T_A = 125^\circ\text{C}$		21		mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^\circ\text{C}$		15		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, $A_V = +1$		22		mA
				4		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V}$ to 55 V $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	150 145	160		dB dB
Supply Current per Amplifier	I_{SY}	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		830	900 950	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		1.8		V/ μs
	SR-	$R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		0.9		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_{VO} = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_{VO} = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_{VO} = 1$		64		Degrees
Settling Time to 0.1%	t_S	$V_{IN} = 10\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		12		μs
Settling Time to 0.01%	t_S	$V_{IN} = 10\text{ V step}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$, $A_V = 1$		14		μs
Channel Separation	CS	$V_{IN} = 10\text{ V p-p}$, $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}$, frequency = 400 MHz		72		dB
		$V_{IN} = 100\text{ mV}_{PEAK}$, frequency = 900 MHz		80		dB
		$V_{IN} = 100\text{ mV}_{PEAK}$, frequency = 1800 MHz		83		dB
		$V_{IN} = 100\text{ mV}_{PEAK}$, frequency = 2400 MHz		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	$A_V = +1$, frequency = 1 kHz, $V_{IN} = 6\text{ V rms}$		0.0005		%
Bandwidth = 80 kHz				0.004		%
Bandwidth = 500 kHz						
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100$, frequency = 0.1 Hz to 10 Hz		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100$, frequency = 1 kHz		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100$, frequency = 0.1 Hz to 10 Hz		16		pA p-p
Current Noise Density	i_N	$A_V = 100$, frequency = 1 kHz		0.8		pA/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—55 V OPERATION

$V_{SY} = 55\text{ V}$, $V_{CM} = V_{SY}/2\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.5	7	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			6	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	150	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		80	300	pA
Input Voltage Range	IVR		0		53.5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 53.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	140	144		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to } 54.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	135	137		dB
Input Resistance						
Differential Mode	R_{INDM}			30		$\text{k}\Omega$
Common Mode	R_{INCM}			1000		$\text{G}\Omega$
Input Capacitance						
Differential Mode	C_{INDM}			7		pF
Common Mode	C_{INCM}			35		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega\text{ to } V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	54.75	54.8		V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega\text{ to } V_{SY}/2$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	54.65	200	250	mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		14	350	mA
Short-Circuit Current Source	I_{SC+}	$T_A = 125^\circ\text{C}$		21		mA
Short-Circuit Current Sink	I_{SC-}	$T_A = 125^\circ\text{C}$		15		mA
Closed-Loop Output Impedance	Z_{OUT}	Frequency = 1 MHz, $A_v = +1$		32		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 4.5\text{ V to } 55\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	150	160		dB
Supply Current per Amplifier	I_{SY}	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	145	830	900	μA
					950	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR+	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		1.7		V/ μ s
	SR-	$R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		0.8		V/ μ s
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_{VO} = 100$		2.7		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_{VO} = 1$		3		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3\text{ dB}}$	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		6.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_{VO} = 1$		64		Degrees
Settling Time to 0.1%	t_s	$V_{IN} = 10\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		12		μ s
Settling Time to 0.01%	t_s	$V_{IN} = 10\text{ V step}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}, A_V = 1$		14		μ s
Channel Separation	CS	$V_{IN} = 10\text{ V p-p}, f = 10\text{ kHz}, R_L = 10\text{ k}\Omega, C_L = 50\text{ pF}$		98		dB
EMI Rejection Ratio of +IN x	EMIRR	$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 400\text{ MHz}$		72		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 900\text{ MHz}$		80		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 1800\text{ MHz}$		83		dB
		$V_{IN} = 100\text{ mV}_{PEAK}, \text{ frequency} = 2400\text{ MHz}$		85		dB
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD + N	$A_V = +1, \text{ frequency} = 1\text{ kHz}, V_{IN} = 10\text{ V rms}$		0.0007		%
				0.003		%
Peak-to-Peak Voltage Noise	$e_{N\text{ p-p}}$	$A_V = 100, \text{ frequency} = 0.1\text{ Hz to }10\text{ Hz}$		117		nV p-p
Voltage Noise Density	e_N	$A_V = 100, \text{ frequency} = 1\text{ kHz}$		5.8		nV/ $\sqrt{\text{Hz}}$
Peak-to-Peak Current Noise	$i_{N\text{ p-p}}$	$A_V = 100, \text{ frequency} = 0.1\text{ Hz to }10\text{ Hz}$		16		pA p-p
Current Noise Density	i_N	$A_V = 100, \text{ frequency} = 1\text{ kHz}$		0.8		pA/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	60 V
Input Voltage Range	(V-) – 300 mV to (V+) + 300 mV
Input Current ¹	±10 mA
Differential Input Voltage	±5 V
Output Short-Circuit Duration to Ground	Indefinite
Temperature Range	
Storage	–65°C to +150°C
Operating	–40°C to +125°C
Junction	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ The input pins have clamp diodes connected to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

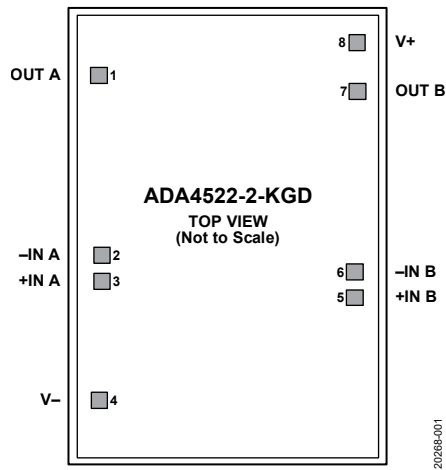


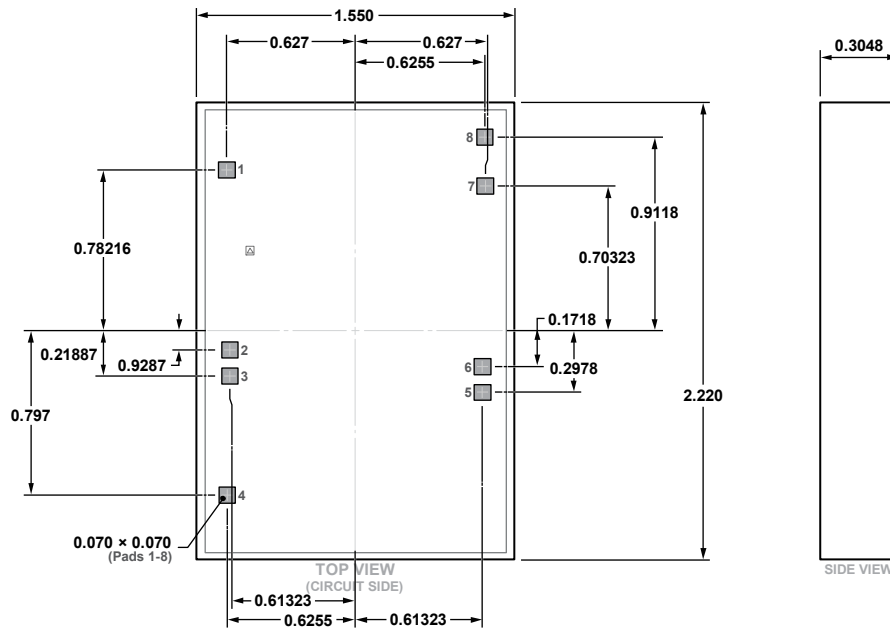
Figure 1. Pad Configuration

Table 5. Pad Function Descriptions¹

Pad Number	Mnemonic	X Coordinate	Y Coordinate	Description
1	OUT A	-627	+782	Output, Channel A
2	-IN A	-613	-93	Inverting Input, Channel A
3	+IN A	-613	-219	Noninverting Input, Channel A
4	V-	-626	-797	Negative Supply Voltage
5	+IN B	+613	-298	Noninverting Input, Channel B
6	-IN B	+613	-172	Inverting Input, Channel B
7	OUT B	+627	+703	Output, Channel B
8	V+	+626	+944	Positive Supply Voltage

¹ All dimensions are referenced from the center of the die to the center of each bond pad.

OUTLINE DIMENSIONS



11-01-2018-A

Figure 2. 8-Pad Bare Die [CHIP]
(C-8-17)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1470 × 2140	μm
Scribe Line Width	80 × 80	μm
Die Size	1550 × 2220	μm
Thickness	305	μm
Backside	V- or left floating	V
Passivation	10 kA high density plasma oxide + 7 kA nitride	Not applicable
Bond Pads (Minimum)	70 × 70	μm
Bond Pad Composition	0.5 Aluminum (Al), copper (Cu)	%

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Hitachi CEL 9240HF10AK
Bonding Method	1 mil gold
Bonding Sequence	Unspecified

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADA4522-2-KGD-WP	-40°C to +125°C	8-Pad Bare Die [CHIP], Waffle Pack	C-8-17

¹ Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

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