High Temperature, 16-Bit, Unbuffered Voltage Output DAC, SPI Interface

Data Sheet **AD5600**

FEATURES

High temperature operation: −55°C to +175°C
16-bit resolution
Fully monotonic
3-wire SPI
Power-on reset feature
Hardware $\overline{\text{LDAC}}$ feature
2.7 V to 5.5 V single-supply operation
Small footprint
10-lead, 3 mm × 3 mm, monometallic wire bonding MSOP
1.8 V logic compatible

APPLICATIONS

Downhole drilling and instrumentation
Heavy industrial
High temperature environments

FUNCTIONAL BLOCK DIAGRAM

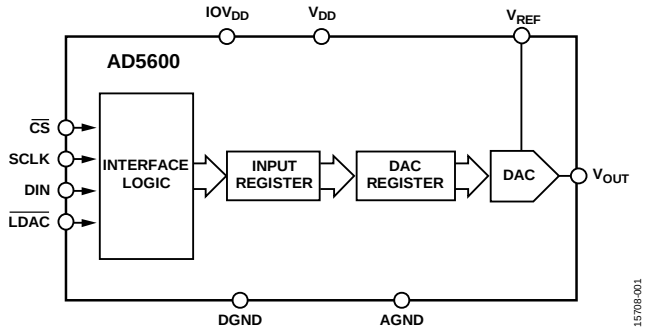

Figure 1.

GENERAL DESCRIPTION

The AD5600 is a single channel, 16-bit resolution, voltage output digital-to-analog converter (DAC) designed for high temperature operation.

The AD5600 guarantees 16-bit monotonicity over the specified temperature range and operates from a single 2.7 V to 5.5 V voltage supply.

For space constrained applications, the AD5600 is available in a 10-lead MSOP with operation specified from −55°C to +175°C. This package is designed for robustness at extreme temperatures, including monometallic wire bonding, and is qualified for up to 1000 hours of operation at the maximum temperature rating.

The AD5600 uses a versatile 3-wire serial peripheral interface (SPI) that is compatible with 50 MHz SPI, QSPI™, MICROWIRE™, and DSP interface standards.

The AD5600 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

PRODUCT HIGHLIGHTS

1. 16-bit monotonic DAC
2. 2.7 V to 5.5 V single-supply operation
3. 1.8 V logic compatible
4. Wide operating temperature range: −55°C to +175°C

Rev. A **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

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10/2019—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, IOV_{DD} = 1.8 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V, and T_A = −55°C to +175°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution		16			Bit
Relative Accuracy (INL)			±0.5	±17	LSB
Differential Nonlinearity (DNL)	Guaranteed monotonic		±0.5	±1.0	LSB
Zero-Scale Error			0.3	±16	LSB
Temperature Coefficient			±0.05		ppm/°C
Gain Error			0.5	±22	LSB
Temperature Coefficient			±0.1		ppm/°C
DC Power Supply Rejection Ratio (PSRR)				±1.2	LSB
OUTPUT CHARACTERISTICS					
Voltage Range		0		V_{REF} − 1 LSB	V
Impedance			6.25		kΩ
VOLTAGE REFERENCE INPUT					
Impedance		9			kΩ
Range		2		V_{DD}	V
Capacitance			26		pF
LOGIC INPUTS					
Input Current				±1.0	µA
Input Voltage					
Low (V_{INL})	IOV_{DD} = 1.65 V to 5.5 V			0.4	V
	IOV_{DD} = 2.7 V to 5.5 V			0.8	V
High (V_{INH})	IOV_{DD} = 1.65 V to 5.5 V	1.3			V
	IOV_{DD} = 2.7 V to 5.5 V	2.4			V
Pin Capacitance			10		pF
Hysteresis Voltage			0.15		V
POWER REQUIREMENTS					
Power Supply					
V_{DD} Voltage	V_{INH} = IOV_{DD} or V_{INL} = DGND	2.7		5.5	V
IOV_{DD} Voltage	V_{INH} = IOV_{DD} or V_{INL} = DGND	1.65		5.5	V
Analog Current (AI_{DD})			125	130	µA
IOV_{DD} Current (IOI_{DD})			15	24	µA

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, IOV_{DD} = 1.8 V to 5.5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, AGND = DGND = 0 V, and T_A = −55°C to +175°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Condition
OUTPUT VOLTAGE SETTLING TIME		30		µs	To divide the LSB of the full scale in half, load capacitance (C_L) = 18 pF
SLEW RATE		7		V/µs	C_L = 18 pF, measured from 0% to 63%
DIGITAL-TO-ANALOG GLITCH IMPULSE		1.5		nV-sec	1 LSB change around major carry
REFERENCE					
−3 dB Bandwidth		1.2		MHz	All 1s loaded, V_{REF} capacitance (C_{REF}) = 0.1 µF
Feedthrough		1.4		mV p-p	All 0s loaded, V_{REF} = 1 V p-p at 100 kHz
DIGITAL FEEDTHROUGH		0.4		nV-sec	
SIGNAL-TO-NOISE RATIO		95		dB	
SPURIOUS-FREE DYNAMIC RANGE		80		dB	Digitally generated sine wave at 1 kHz
TOTAL HARMONIC DISTORTION		74		dB	DAC code = 0xFFFF, frequency 10 kHz, V_{REF} = 2.5 V ± 1 V p-p
OUTPUT					
Noise Spectral Density		14		nV/√Hz	DAC code = 0x0000, frequency = 1 kHz
Noise		1.25		µV p-p	0.1 Hz to 10 Hz

TIMING CHARACTERISTICS

V_{DD} = 5 V, 2.5 V ≤ V_{REF} ≤ V_{DD}, V_{INH} = 90% of IOV_{DD}, V_{INL} = 10% of IOV_{DD}, AGND = DGND = 0 V, and −55°C < T_A < +175°C, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at 1.62 ≤ IOV_{DD} ≤ 2.7 V	Limit at 2.7 V ≤ IOV_{DD} ≤ 5.5 V	Unit	Description
f_{SCLK}	14	50	MHz max	SCLK cycle frequency
t_1	70	20	ns min	SCLK cycle time
t_2	35	10	ns min	SCLK high time
t_3	35	10	ns min	SCLK low time
t_4	5	5	ns min	$\overline{CS}$ low to SCLK high setup
t_5	5	5	ns min	$\overline{CS}$ high to SCLK high setup
t_6	5	5	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	10	5	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	35	10	ns min	Data setup time
t_9	5	4	ns min	Data hold time (V_{INH} = 90% of IOV_{DD}, V_{INL} = 10% of IOV_{DD})
t_9	5	5	ns min	Data hold time (V_{INH} = 3 V, V_{INL} = 0 V)
t_{10}	20	20	ns min	$\overline{LDAC}$ pulse width
t_{11}	10	10	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup
t_{12}	15	15	ns min	$\overline{CS}$ high time between active periods

[1] Guaranteed by design and characterization. Not production tested.
[2] All input signals are specified with rise time (t_R) = fall time (t_F) = 1 ns/V and timed from a voltage level of (V_{INL} + V_{INH})/2.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +6 V
IOV_{DD} to AGND	−0.3 V to +6 V
Digital Inputs[1] to DGND	−0.3 V to IOV_{DD} + 0.3 V
V_{OUT} to AGND	−0.3 V to V_{DD} + 0.3 V
AGND to DGND	0.3 V
Digital Input Pin Current	±10 mA
Temperature	
Operating Range[2]	−55°C to +175°C
Junction Temperature, T_{JMAX}	175°C
Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Reflow Soldering Peak, Pb Free	260°C
Electrostatic Discharge (ESD)	5 kV

[1] The digital inputs include SCLK, DIN, $\overline{CS}$, and $\overline{LDAC}$.
[2] Qualified for up to 1000 hours of operation at the maximum temperature range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}	Unit
RM-10[1]	146.76	84.21	38.12	2.56	82.41	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

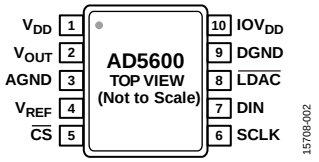

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. The device can operate from 2.7 V to 5.5 V. Decouple V_{DD} to AGND.
2	V_{OUT}	Analog Output Voltage from the DAC.
3	AGND	Analog Ground. Ground reference point for all analog circuitry on the device.
4	V_{REF}	Voltage Reference Input. Connect this pin to an external voltage reference.
5	$\overline{CS}$	Chip Select Input Signal. $\overline{CS}$ frames the serial data input.
6	SCLK	Serial Clock Input Signal. Data is clocked into the serial input register on the rising edge of SCLK.
7	DIN	Serial Data Input Signal. This device accepts 16-bit words. Data is clocked into the serial input register on the rising edge of SCLK.
8	$\overline{LDAC}$	$\overline{LDAC}$ Input Signal. Pulsing this pin low allows the DAC register to be updated if the input register has new data. This pin can be tied permanently low. In this case, the DAC is automatically updated when new data is written to the input register on the rising edge of $\overline{CS}$.
9	DGND	Digital Ground. Ground reference point for all digital circuitry on the device.
10	IOV_{DD}	Digital Interface Supply Voltage. The voltage range is 1.65 V to 5.5 V. Decouple IOV_{DD} to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

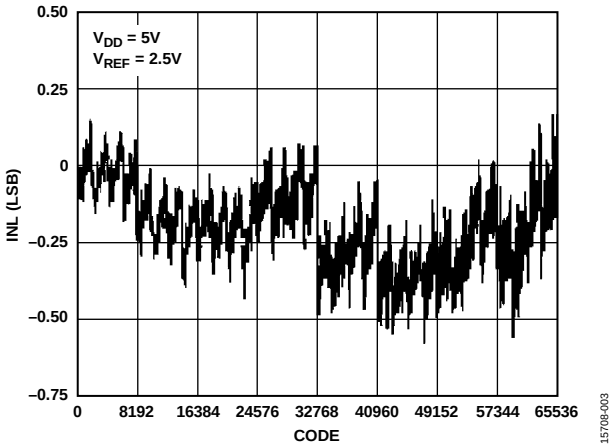

Figure 3. INL vs. Code

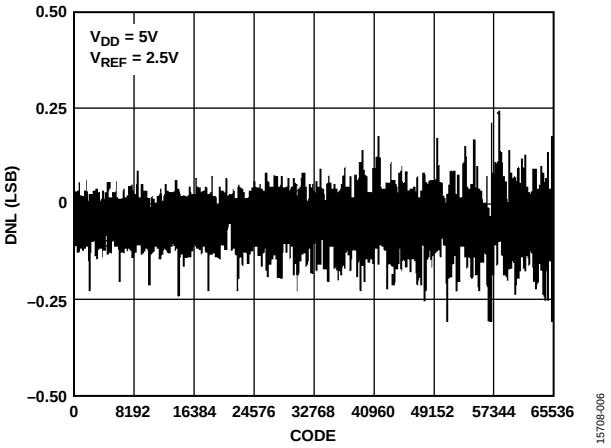

Figure 6. DNL vs. Code

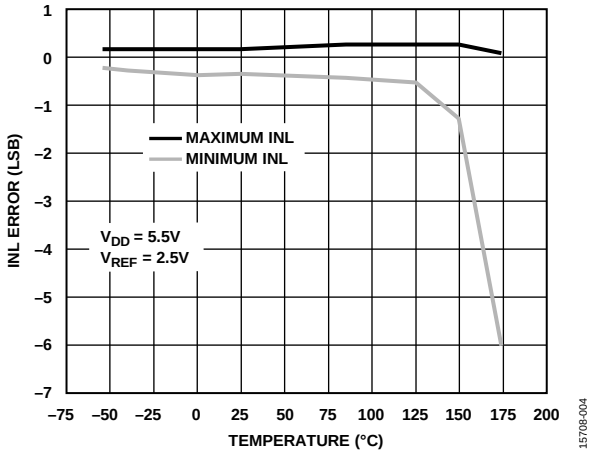

Figure 4. INL Error vs. Temperature

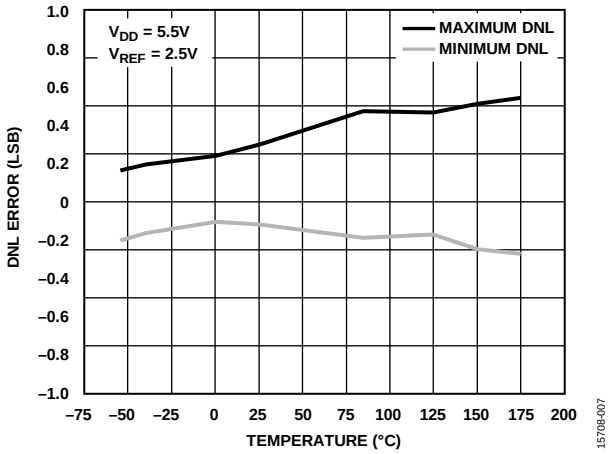

Figure 7. DNL Error vs. Temperature

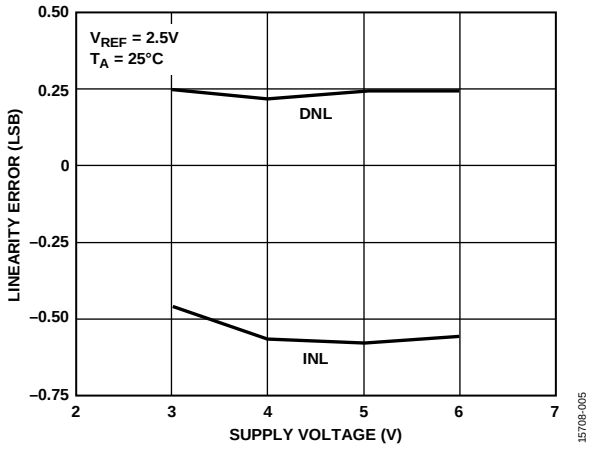

Figure 5. Linearity Error vs. Supply Voltage

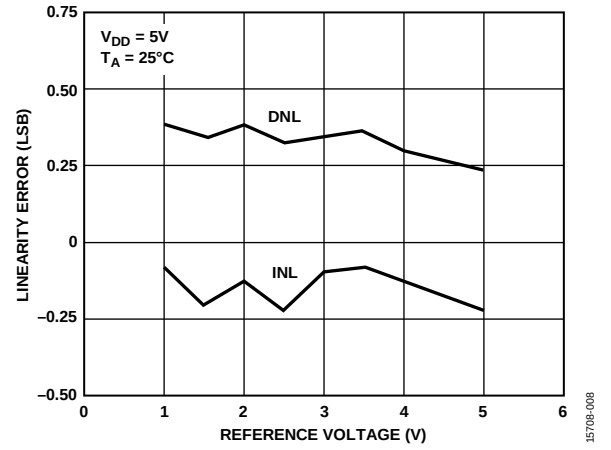

Figure 8. Linearity Error vs. Reference Voltage

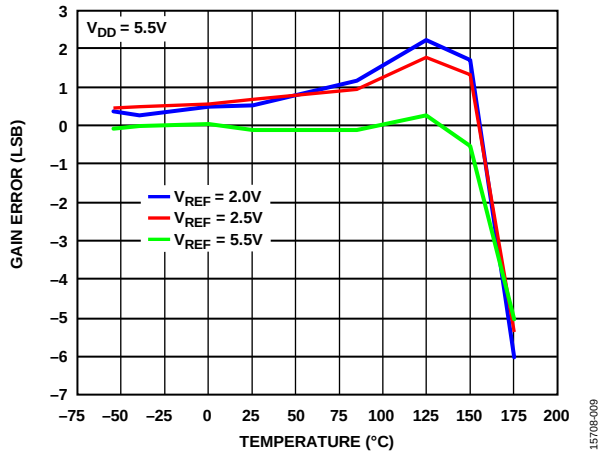

Figure 9. Gain Error vs. Temperature

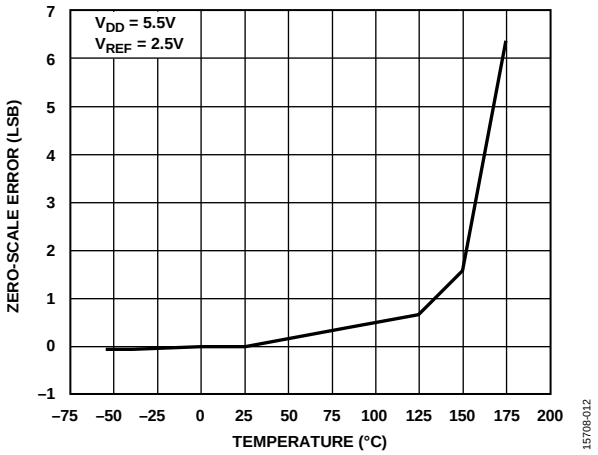

Figure 12. Zero-Scale Error vs. Temperature

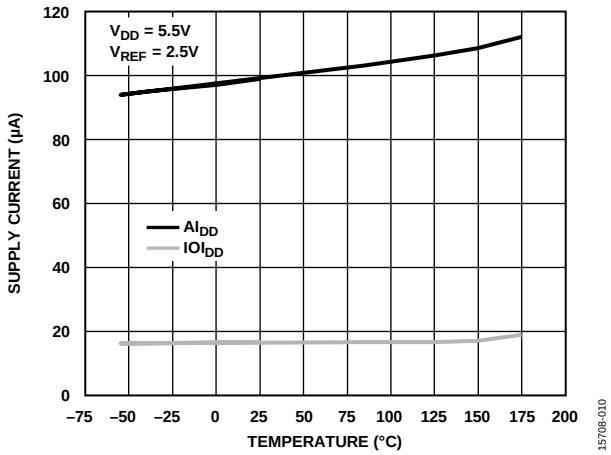

Figure 10. Supply Current vs. Temperature

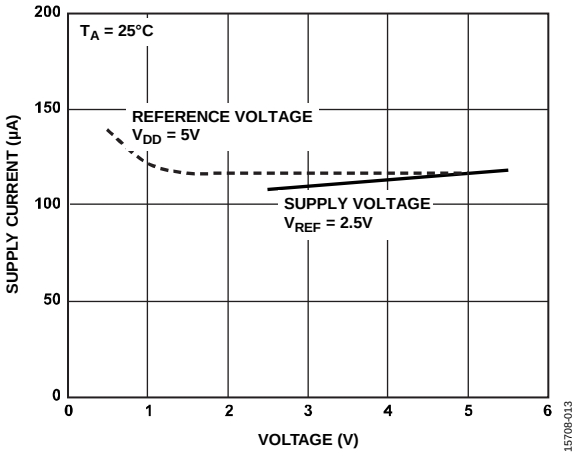

Figure 13. Supply Current vs. Voltage (Reference and Supply)

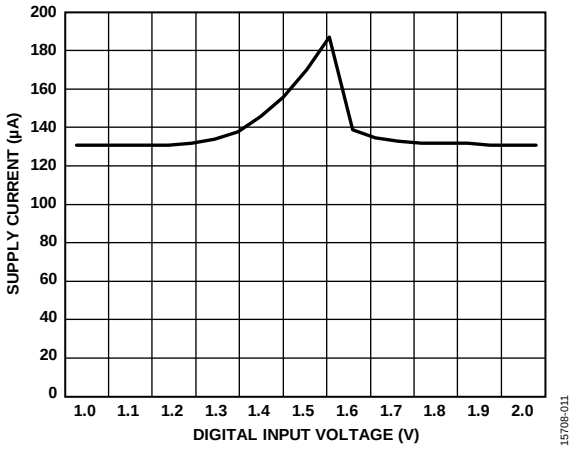

Figure 11. Supply Current vs. Digital Input Voltage

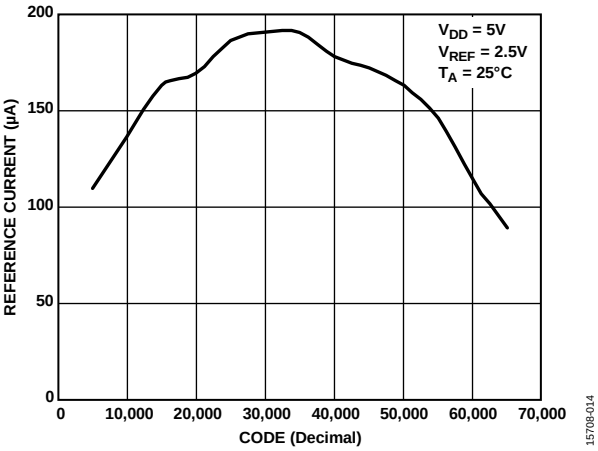

Figure 14. Reference Current vs. Code

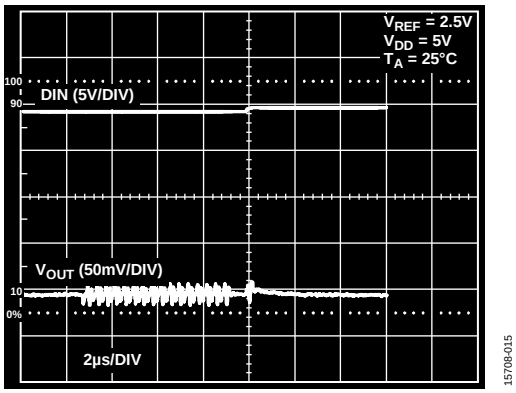

Figure 15. Digital Feedthrough

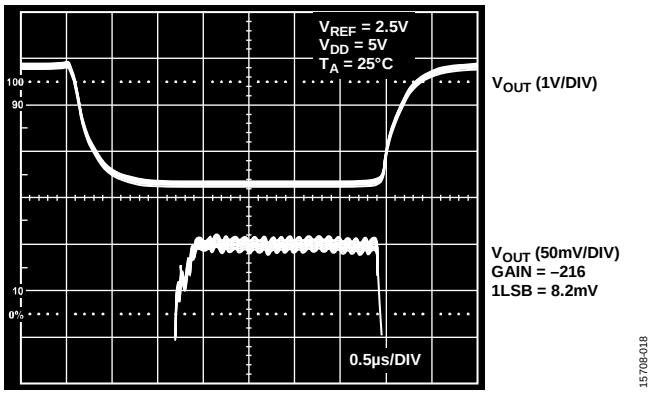

Figure 18. Small Signal Settling Time

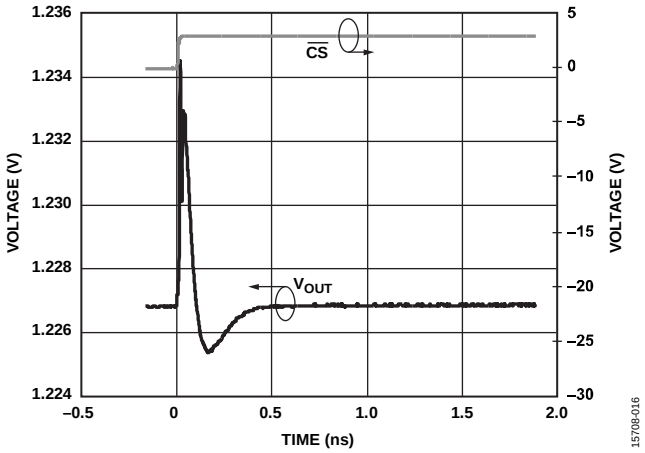

Figure 16. Digital-to-Analog Glitch Impulse

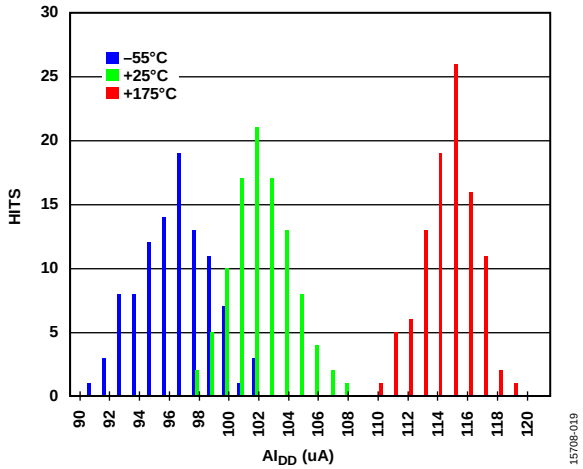

Figure 19. AI_{DD} Histogram

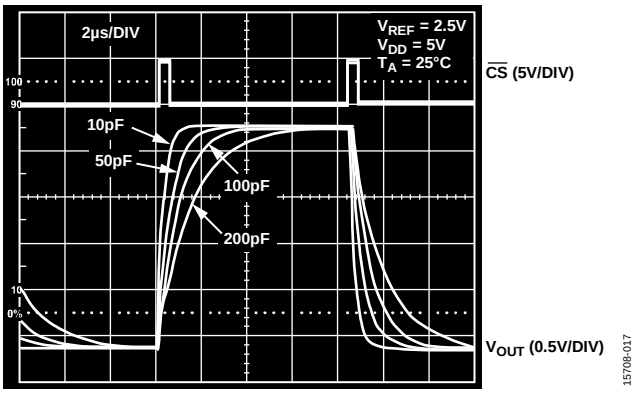

Figure 17. Large Signal Settling Time

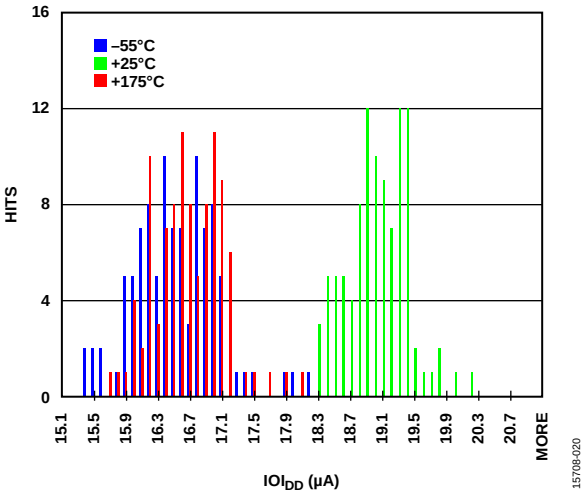

Figure 20. IOI_{DD} Histogram

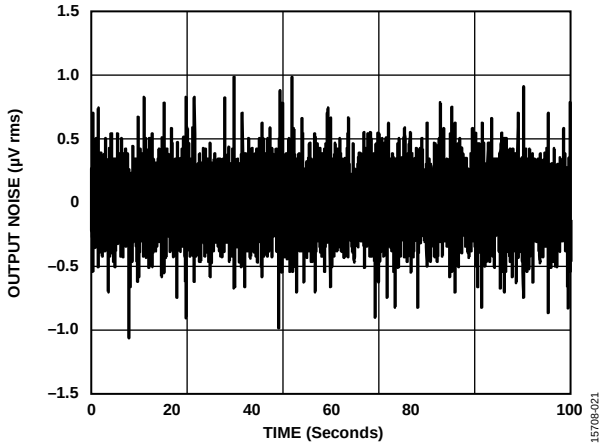

Figure 21. 0.1 Hz to 10 Hz Output Noise

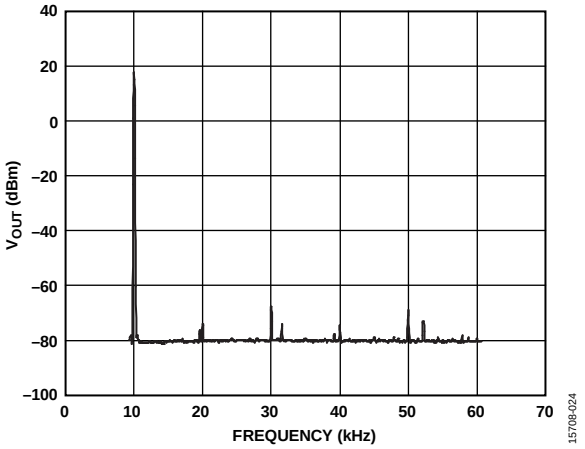

Figure 24. Total Harmonic Distortion

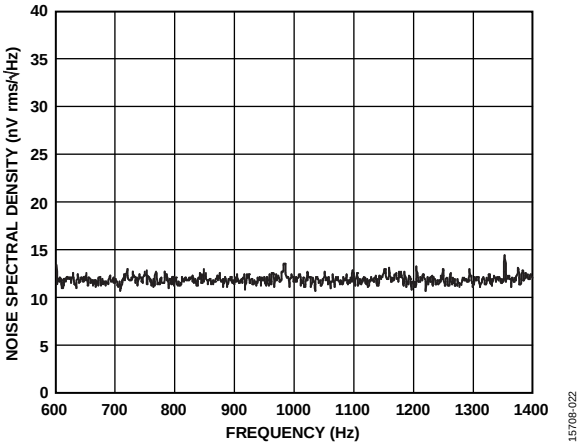

Figure 22. Noise Spectral Density vs. Frequency,1 kHz

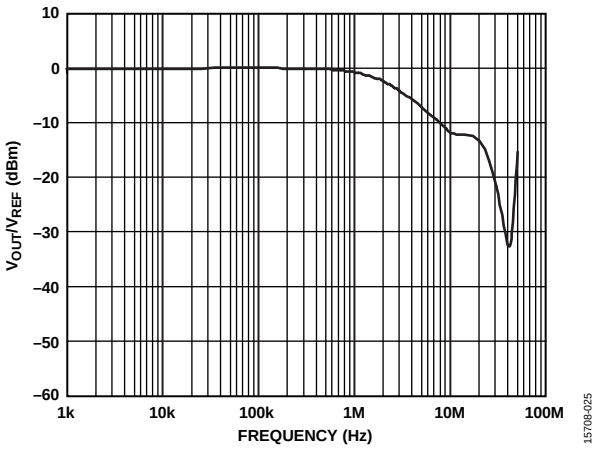

Figure 25. Multiplying Bandwidth

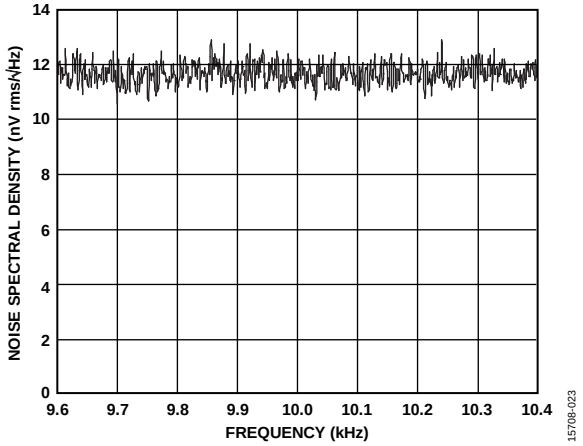

Figure 23. Noise Spectral Density vs. Frequency, 10 kHz

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 3.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. A typical DNL vs. code plot is shown in Figure 6.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as LSB. It is the deviation in slope of the DAC transfer characteristic from the ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. This temperature coefficient is expressed in ppm/°C.

Zero-Scale Error
Zero-scale error is a measure of the output error when zero scale is loaded to the DAC register.

Zero-Scale Temperature Coefficient
Zero-scale temperature coefficient is a measure of the change in zero-scale error with a change in temperature. This temperature coefficient is expressed in ppm/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. This impulse is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A digital-to-analog glitch impulse plot is shown in Figure 16.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC. However, this feedthrough is measured when the DAC output is not updated. $\overline{CS}$ is held high while the SCLK and DIN signals are toggled. Digital feedthrough is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical digital feedthrough plot is shown in Figure 15.

DC Power Supply Rejection Ratio (PSRR)
DC PSRR indicates how the output of the DAC is affected by changes in the power supply voltage. The DC power supply rejection ratio is expressed in terms of the LSB number change in the output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
Reference feedthrough is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

THEORY OF OPERATION

The AD5600 is a single channel, 16-bit, serial input, voltage output DAC designed for high temperature operation. The device operates from a supply voltage range of 2.7 V to 5.5 V.

The AD5600 input shift register is 16 bits wide. Data is written to the device through the 3-wire SPI at clock speeds up to 50 MHz.

The AD5600 incorporates a power-on reset circuit that ensures that the DAC output register powers up to a known state.

DAC

DAC Architecture

The DAC architecture consists of two matched DAC sections. A simplified circuit architecture is shown in Figure 26. The DAC architecture of the AD5600 is segmented. The four MSBs of the 16-bit DAC word drive are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors to either AGND or V_{REF}. The remaining twelve bits of the DAC word drive switch S0 to S11 of a 12-bit voltage mode R-2R ladder network.

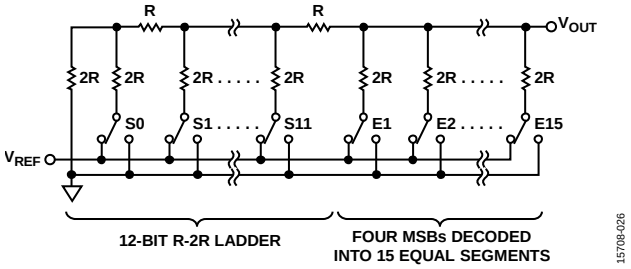

Figure 26. Simplified DAC Architecture

Transfer Function

The input coding to the DAC is straight binary. The ideal output voltage is given by

$$V_{OUT} = V_{REF} \times (D/65{,}536)$$

where:
D is the decimal equivalent of the binary code that is loaded into the DAC register.

SERIAL INTERFACE

The AD5600 uses a 3-wire serial interface that is compatible with SPI, QSPI, MICROWIRE and DSP interface standards. The serial interface can operate at clock rates up to 50 MHz.

The AD5600 has a 16-bit wide input shift register. When writing to the input shift register, the $\overline{CS}$ pin frames the SPI transaction. A high to low transition on the $\overline{CS}$ pin starts a write transaction, and a low to high transition on the $\overline{CS}$ pin ends the transaction. Data is loaded into the input shift register, MSB first, on the rising edge of the serial clock (SCLK).

If more than 16 bits of data are loaded to the input shift register, the last 16 bits are kept. If less than 16 bits of data are loaded, bits remain from the previous word loaded in.

HARDWARE $\overline{LDAC}$

The AD5600 features a hardware $\overline{LDAC}$ pin that can control the transfer of data from the input shift register to the DAC register.

Instantaneous Updating

If $\overline{LDAC}$ is held low on the falling edge of $\overline{CS}$ during a SPI write transaction, the DAC register is updated with the contents of the input register on the rising edge of $\overline{CS}$ at the end of the frame.

Deferred Updating

If $\overline{LDAC}$ is held high during a SPI write frame, the contents of the input register are not transferred into the DAC register until a falling edge is detected on the $\overline{LDAC}$ pin. Falling edges on the $\overline{LDAC}$ pin are ignored while the $\overline{CS}$ pin is low.

POWER-ON RESET

The AD5600 has a power-on reset circuit that ensures that the DAC output powers up to a known state. On power-up, the content of the AD5600 DAC register is cleared to all 0s. This register remains in this state until the user loads data from the input register. The input register of the AD5600 is not cleared on power-up. When initially loading data into the DAC, at least 16 bits of data must be loaded to the DAC to overwrite the undefined data from power-up.

If $\overline{LDAC}$ is held low on power-up, a low to high transition on $\overline{CS}$ may transfer the erroneous contents in the input register to the DAC register. Clear the input register contents before bringing $\overline{CS}$ high.

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5600 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5600 is in a system where multiple devices require an analog ground to digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The AD5600 must have 10 µF supply bypassing capacitors in parallel with 0.1 µF capacitors on each supply located as close to the package as possible, ideally right up against the device. It is recommended to use 10 µF tantalum bead capacitors. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, to provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

DECODING MULTIPLE DACs

The $\overline{CS}$ pin of the AD5600 can select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time. The DAC addressed is determined by the decoder. Some digital feedthrough from the digital input lines exists. Use a burst clock to minimize the effects of digital feedthrough on the analog signal channels. Figure 27 shows a typical circuit.

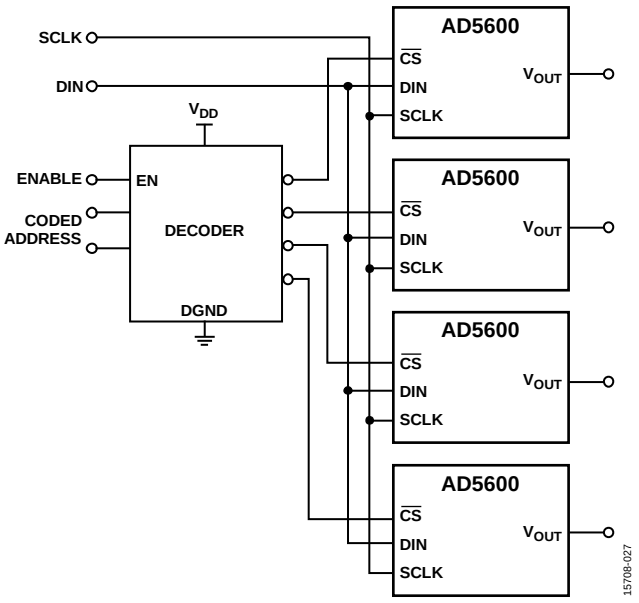

Figure 27. Addressing Multiple DACs

OUTLINE DIMENSIONS

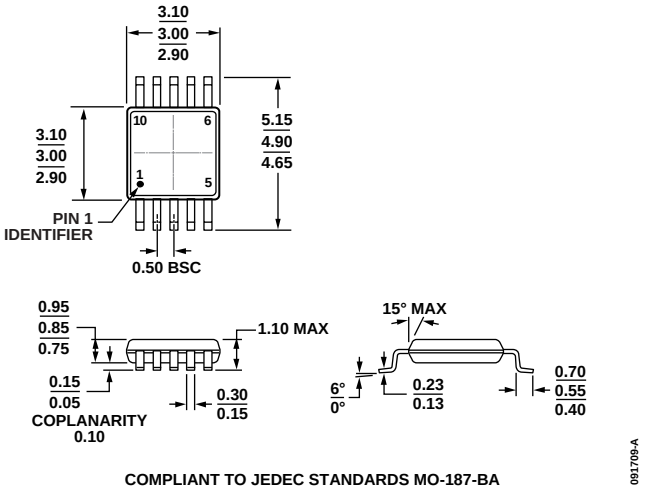

Figure 28. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5600HRMZ	−55°C to +175°C	10-Lead Mini Small Outline Package [MSOP]	RM-10
EVAL-AD5600PMDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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