

# EN55022B Compliant 58V, 24W Inverting-Output DC/DC $\mu$ Module Regulator

## FEATURES

- Complete Low EMI Switch Mode Power Supply
- EN55022 Class B Compliant
- Wide Input Voltage Range: 3.6V to 58V
- Up to 4A Output Current
  - 24W Output from 12V<sub>IN</sub> to -24V<sub>OUT</sub>, P<sub>LOSS</sub> = 5W, T<sub>A</sub> = 60°C, t<sub>RISE</sub> = 60°C, 200LFM
- Output Voltage Range: -26.5V ≤ V<sub>OUT</sub><sup>-</sup> ≤ -0.5V
  - Safe Operating Area: V<sub>IN</sub> + |V<sub>OUT</sub><sup>-</sup>| ≤ 58V
- ±1.67% Total DC Output Voltage Error Over Line, Load and Temperature (-40°C to 125°C)
- Parallel and Current Share with Multiple LTM4651s
- Constant-Frequency Current Mode Control
- Frequency Synchronization Range: 250kHz to 3MHz
- Power Good Indicator and Programmable Soft-Start
- Overcurrent/Overvoltage/Overtemperature Protection
- 15mm × 9mm × 5.01mm BGA Package

## APPLICATIONS

- Avionics, Industrial Control and Test Equipment
- Video, Imaging and Instrumentation
- 48V Telecom and Network Power Supplies
- RF Systems

## DESCRIPTION

The LTM<sup>®</sup>4651 is an ultralow noise, 58V, 24W DC/DC  $\mu$ Module<sup>®</sup> inverting topology regulator. It regulates a negative output voltage (V<sub>OUT</sub><sup>-</sup>) from a positive input supply voltage (V<sub>IN</sub>), and is designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power MOSFETs, inductor, filters and support components.

The LTM4651 can regulate V<sub>OUT</sub><sup>-</sup> to a value between -0.5V and -26.5V, provided that its input and output voltages adhere to the safe operating area criteria of the LTM4651: V<sub>IN</sub> + |V<sub>OUT</sub><sup>-</sup>| ≤ 58V. A switching frequency range of 250kHz to 3MHz is supported (400kHz default) and the module can synchronize to an external clock.

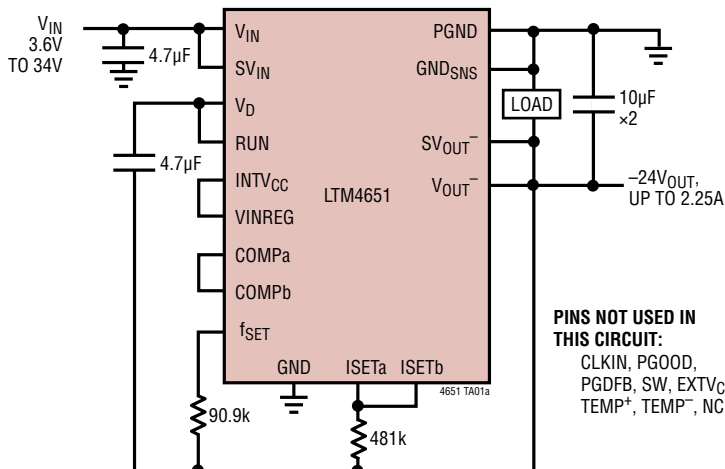
Despite being an inverting topology regulator, no level shift circuitry is needed to interface to the LTM4651's RUN, PGOOD or CLKIN pins; those pins are referenced to GND.

The LTM4651 is offered in a 15mm × 9mm × 5.01mm BGA package with SnPb or RoHS compliant terminal finish.

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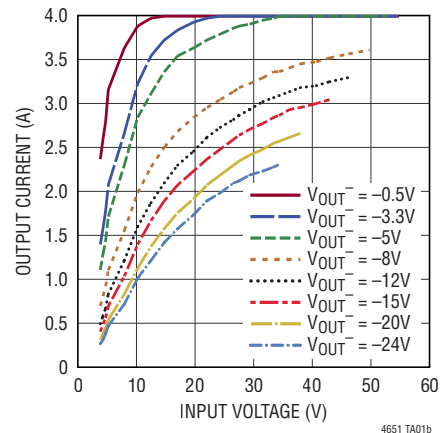
## TYPICAL APPLICATION

-24V, 2.25A\* Ultralow Noise\*\* DC/DC  $\mu$ Module Regulator



\*\*See Figures 5 – 8 for DC2328A Radiated Emission Performance against EN55022B limits.

Output Current Capability\*



\*Current limit frequency-foldback activates at load currents higher than indicated curves. Continuous output current capability subject to details of application implementation. Switching frequency set per Table 1. See Notes 2 and 3.

# LTM4651

## ABSOLUTE MAXIMUM RATINGS

(Note 1) (All Voltages Relative to  $V_{OUT^-}$  Unless Otherwise Indicated)

### Terminal Voltages

$V_{IN}$ , $V_D$ , $SV_{IN}$ , SW, PGND, $GND_{SNS}$ , ISETa ..	-0.3V to 60V
GND, EXT $V_{CC}$ .....	-0.3V to 28V
RUN .....	$GND - 0.3V$ to $V_{OUT^-} + 60V$
INT $V_{CC}$ , PGDFB, VINREG, COMPa .....	-0.3V to 4V
$f_{SET}$ .....	-0.3V to INT $V_{CC}$
COMPb .....	-0.3V to 5V
ISETb .....	-0.3V to 28V
CLKIN, PGOOD (Relative to GND) .....	-0.3V to 6V

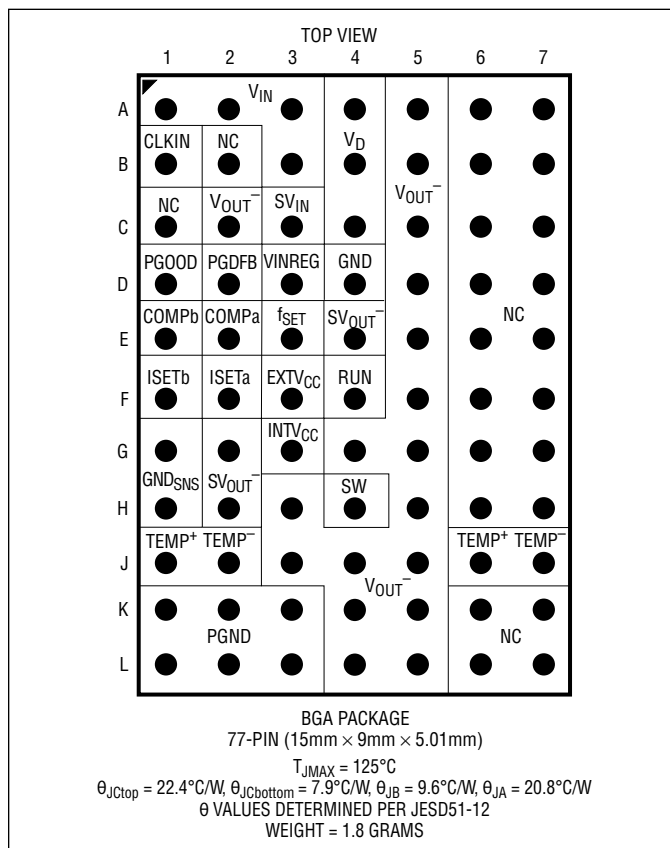
### Terminal Currents

INT $V_{CC}$ Peak Output Current (Note 8) .....	30mA
TEMP $^+$ .....	-1mA to 10mA
TEMP $^-$ .....	-10mA to 1mA

### Temperatures

Internal Operating Temperature	
Range (Notes 2, 7) .....	-40°C to 125°C
Storage Temperature Range .....	
	-55°C to 125°C
Peak Solder Reflow Package	
Body Temperature .....	245°C

## PIN CONFIGURATION



## ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4651EY#PBF	SAC305 (RoHS)	LTM4651Y	e1	BGA	3	-40°C to 125°C
LTM4651IY#PBF			e0			-40°C to 125°C
LTM4651IY	SnPb (63/37)					

• Contact the factory for parts specified with wider operating temperature ranges. \*Pad or ball finish code is per IPC/JEDEC J-STD-609.

- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2).  $T_A = 25^\circ\text{C}$ , Test Circuit 1,  $V_{IN} = 24\text{V}$  and electrically connected to  $SV_{IN}$  and RUN,  $ISETa - SV_{OUT}^- = 24\text{V}$ ,  $EXTV_{CC} = PGND$ , CLKIN open circuit,  $R_{fSET} = 57.6\text{k}\Omega$  and  $R_{iSET} = 480\text{k}\Omega$  and voltages referred to PGND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$SV_{IN(DC)}, V_{IN(DC)}$	Input DC Voltage	$V_{IN}^+  V_{OUT}^-  \leq 58\text{V}$	●	3.6	58	V	
$V_{OUT(RANGE)}^-$	Range of Output Voltage Regulation	$0.5\text{V} \leq ISETa - SV_{OUT}^- \leq 26.5\text{V}$	●	-26.5	-0.5	V	
$V_{OUT(-24VDC)}^-$	Output Voltage Total Variation with Line and Load at $V_{OUT}^- = -24\text{V}$	$3.6\text{V} \leq V_{IN} \leq 34\text{V}$ , $0\text{A} \leq I_{OUT}^- \leq 0.3\text{A}$ , CLKIN Driven per Note 6, $C_{INH} = 4.7\mu\text{F}$ , $C_D = 4.7\mu\text{F} \times 2$ , $C_{OUTH} = 47\mu\text{F} \times 2$	●	-24.4	-24	-23.6	V
$V_{OUT(-5VDC)}^-$	Output Voltage Total Variation with Line and Load at $V_{OUT}^- = -5\text{V}$	Measuring $GND_{SNS} - ISETa$ $12\text{V} \leq V_{IN} \leq 53\text{V}$ , $0\text{A} \leq I_{OUT}^- \leq 3\text{A}$ , CLKIN Driven by 550kHz Clock, $C_{INH} = 4.7\mu\text{F}$ , $C_D = 4.7\mu\text{F} \times 2$ , $C_{OUTH} = 47\mu\text{F} \times 2$ , $ISETa - SV_{OUT}^- = 5\text{V}$	●	-15	0	15	mV
$V_{OUT(-0.5VDC)}^-$	Output Voltage Total Variation with Line and Load at $V_{OUT}^- = -0.5\text{V}$	Measuring $GND_{SNS} - ISETa$ $3.6\text{V} \leq V_{IN} \leq 28\text{V}$ , $0\text{A} \leq I_{OUT}^- \leq 2\text{A}$ , $C_{INH} = 4.7\mu\text{F}$ , $C_D = 4.7\mu\text{F} \times 2$ , $C_{OUTH} = 47\mu\text{F} \times 2$ , $R_{fSET} = N/U$ , $ISETa - SV_{OUT}^- = 500\text{mV}$ , CLKIN Driven by 200kHz Clock (Note 5)	●	-15	0	15	mV

#### Input Specifications

$V_{IN(UVLO)}$	$SV_{IN}$ Undervoltage Lockout Threshold	$SV_{IN}$ Rising $SV_{IN}$ Falling Hysteresis	● ● ●	2.1 400	3.2 2.5 700	3.6 2.8	V V mV
$V_{IN(OVLO)}$	$SV_{IN}$ Overvoltage Lockout Rising	(Note 4)		64	68		V
$V_{IN(HYS)}$	$SV_{IN}$ Overvoltage Lockout Hysteresis	(Note 4)			2	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	$C_{INH} = 4.7\mu\text{F}$ , $C_D = 4.7\mu\text{F} \times 2$ , $C_{OUTH} = 47\mu\text{F} \times 2$ ; $I_{OUT}^- = 0\text{A}$ , $ISETa$ Electrically Connected to $ISETb$			1.1		A
$I_Q(SVIN)$	Input Supply Bias Current	Shutdown, RUN = GND RUN = $V_{IN}$			16 450	30	$\mu\text{A}$ $\mu\text{A}$
$I_S(VIN)$	Input Supply Power Converter	CLKIN Open Circuit, $I_{OUT}^- = 2\text{A}$			2.3		A
$I_S(VIN, SHUTDOWN)$	Input Supply Current in Shutdown	Shutdown, RUN = GND			4		$\mu\text{A}$

#### Output Specifications

$I_{OUT}^-$	$V_{OUT}^-$ Output Continuous Current Range	From $V_{IN} = 24\text{V}$ , Regulating $V_{OUT}^- = -24\text{V}$ at $f_{SW} = 1.5\text{MHz}$ From $V_{IN} = 12\text{V}$ , Regulating $V_{OUT}^- = -5\text{V}$ at $f_{SW} = 550\text{kHz}$ (See Note 3, Capable of Up to 4A Output Current for Some Combinations of $V_{IN}$ , $V_{OUT}^-$ , and $f_{SW}$ )		0 0	2 3		A A
$\Delta V_{OUT(LINE)}^- / V_{OUT}^-$	Line Regulation Accuracy	$I_{OUT}^- = 0\text{A}$ , $3.6\text{V} \leq V_{IN} \leq 34\text{V}$ , $ISETa - SV_{OUT}^- = 24\text{V}$ , CLKIN Driven by 1.8MHz Clock	●		0.05	0.25	%
$\Delta V_{OUT(LOAD)}^- / V_{OUT}^-$	Load Regulation Accuracy	$V_{IN} = 24\text{V}$ , $0\text{A} \leq I_{OUT}^- \leq 2\text{A}$ , CLKIN Driven by 1.5MHz Clock, $R_{fSET} = 57.6\text{k}\Omega$ , and $R_{iSET} = 480\text{k}\Omega$	●		0.05	0.5	%
$V_{OUT(AC)}^-$	Output Voltage Ripple, $V_{OUT}^-$	$V_{IN} = 12\text{V}$ , $ISETa - SV_{OUT}^- = 5\text{V}$			10		mV <sub>p-p</sub>
$f_s$	$V_{OUT}$ Ripple Frequency	$V_{IN} = 12\text{V}$ , $ISETa - SV_{OUT}^- = 5\text{V}$	●	1.7	1.95	2.2	MHz
$\Delta V_{OUT(START)}^-$	Turn-On Overshoot				8		mV
$t_{START}$	Turn-On Start-Up Time	Delay Measured from $V_{IN}$ Toggling from 0V to 24V to PGOOD Exceeding 3V Above GND; PGOOD Having a 100k $\Omega$ Pull-Up to 3.3V with Respect to GND, VPGFB Resistor-Divider Network as Shown in Test Circuit 1, $R_{iSETa} = 480\text{k}\Omega$ , $ISETa$ Electrically Connected to $ISETb$ , and CLKIN Driven with 1.2MHz Clock	●		4	9	ms
$\Delta V_{OUT(LS)}^-$	Peak Output Voltage Deviation for Dynamic Load Step	$I_{OUT}^-$ : 0A to 1A and 1A to 0A Load Steps in 1 $\mu\text{s}$ , $C_{OUTH} = 47\mu\text{F} \times 2$ X5R			400		mV
$t_{SETTLE}$	Settling Time for Dynamic Load Step	$I_{OUT}^-$ : 0A to 0.5A and 0.5A to 0A Load Steps in 1 $\mu\text{s}$ , $C_{OUTH} = 47\mu\text{F} \times 2$ X5R			50		$\mu\text{s}$

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2).  $T_A = 25^\circ\text{C}$ , Test Circuit 1,  $V_{IN} = 24\text{V}$  and electrically connected to  $SV_{IN}$  and RUN,  $I_{SETa} - SV_{OUT}^- = 24\text{V}$ ,  $EXTV_{CC} = \text{PGND}$ , CLKIN open circuit,  $R_{fSET} = 57.6\text{k}\Omega$  and  $R_{ISET} = 480\text{k}\Omega$  and voltages referred to PGND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{OUT(OC)}^-$	$I_{OUT}^-$ Output Current Limit			2.45		A
<b>Control Section</b>						
$I_{ISETa}$	Reference Current of ISETa Pin	$V_{ISETa} - SV_{OUT}^- = 0.5\text{V}$ , $3.6\text{V} \leq V_{IN} \leq 28\text{V}$ $0.1\text{V} \leq V_{ISETa} - SV_{OUT}^- \leq V_{IN} - SV_{OUT}^- \leq 58\text{V}$	● ●	49.3 49	50 50	50.7 51 $\mu\text{A}$ $\mu\text{A}$
$I_{GND\SNS}$	$GND_{\text{SNS}}$ Leakage Current	$V_{IN} - SV_{OUT}^- = SV_{IN} - SV_{OUT}^- = \text{RUN} - GND = I_{SETa} - SV_{OUT}^- = 58\text{V}$		600		$\mu\text{A}$
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)		60		ns
$V_{RUN}$	RUN Turn-On/Off Thresholds	RUN Input Turn-On Threshold, RUN Rising RUN Hysteresis (RUN Thresholds Measured with Respect to GND)	●	1.08	1.2 130	V mV
$I_{RUN}$	RUN Leakage Current	$V_{IN} = 48\text{V}$ , $\text{RUN} - GND = 3.3\text{V}$	●	0.1	50	nA
<b>Oscillator and Phase-Locked Loop (PLL)</b>						
$f_{OSC}$	Oscillator Frequency Accuracy	$V_{IN} = 12\text{V}$ , $I_{SETa} - SV_{OUT}^- = 5\text{V}$ , and: $f_{SET}$ Open Circuit $R_{fSET} = 57.6\text{k}\Omega$ (See $f_s$ Specification)	●	360	400 1.95	440  kHz MHz
$f_{SYNC}$	PLL Synchronization Capture Range	$V_{IN} = 12\text{V}$ , $I_{SETa} - SV_{OUT}^- = 5\text{V}$ , CLKIN Driven with a GND-Referred Clock Toggling from 0.4V to 1.2V and Having a Clock Duty Cycle: From 10% to 90%; $f_{SET}$ Open Circuit From 40% to 60%; $R_{fSET} = 57.6\text{k}\Omega$		250 1.3	550 3	kHz MHz
$V_{CLKIN}$	CLKIN Input Threshold	$V_{CLKIN}$ Rising, with Respect to GND $V_{CLKIN}$ Falling, with Respect to GND		1.2	0.4	V V
$I_{CLKIN}$	CLKIN Input Current	$V_{CLKIN} = 5\text{V}$ with Respect to GND $V_{CLKIN} = 0\text{V}$ with Respect to GND		-20	230 -5	500  $\mu\text{A}$ $\mu\text{A}$
<b>Power Good Feedback Input and Power Good Output</b>						
$OV_{PGDFB}$	Output Overvoltage PGOOD Upper Threshold	PGDFB Rising, Differential Voltage from PGDFB to $SV_{OUT}^-$	●	620	645	675 mV
$UV_{PGDFB}$	Output Undervoltage PGOOD Lower Threshold	PGDFB Falling, Differential Voltage from PGDFB to $SV_{OUT}^-$	●	525	555	580 mV
$\Delta V_{PGDFB}$	PGOOD Hysteresis	PGDFB Returning		8		mV
$R_{PGDFB}$	Resistor Between PGDFB and $SV_{OUT}^-$			4.94	4.99	5.04 k $\Omega$
$R_{PGOOD}$	PGOOD Pull-Down Resistance	$V_{PGOOD} = 0.1\text{V}$ with Respect to GND, $V_{PGDFB} - SV_{OUT}^- < UV_{PGDFB}$ or $V_{PGDFB} - SV_{OUT}^- > OV_{PGDFB}$		700	1500	$\Omega$
$I_{PGOOD(LEAK)}$	PGOOD Leakage Current	$V_{PGOOD} = 3.3\text{V}$ with Respect to GND, $UV_{PGDFB} < V_{PGDFB} - SV_{OUT}^- < OV_{PGDFB}$		0.1	1	$\mu\text{A}$
$t_{PGOOD(DELAY)}$	PGOOD Delay	PGOOD Low to High (Note 4) PGOOD High to Low (Note 4)		16/ $f_{SW(HZ)}$ 64/ $f_{SW(HZ)}$		s s

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2).  $T_A = 25^\circ\text{C}$ , Test Circuit 1,  $V_{IN} = 24\text{V}$  and electrically connected to  $SV_{IN}$  and RUN,  $ISETa - SV_{OUT}^- = 24\text{V}$ ,  $EXTV_{CC} = \text{PGND}$ , CLKIN open circuit,  $R_{fSET} = 57.6\text{k}\Omega$  and  $R_{iSET} = 480\text{k}\Omega$  and voltages referred to PGND unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Input Voltage Regulation Pin</b>						
$V_{VINREG}$	VINREG Servo Voltage	VINREG Voltage During Output Current Regulation, Measured with Respect to $SV_{OUT}^-$	● 1.8	2.0	2.2	V
$I_{VINREG}$	VINREG Leakage Current	$VINREG - SV_{OUT}^- = 2\text{V}$		1		nA
<b>INTV<sub>CC</sub> Regulator</b>						
$V_{INTVCC}$	Channel Internal $V_{CC}$ Voltage, No INTV <sub>CC</sub> Loading ( $I_{INTVCC} = 0\text{mA}$ )	$3.6\text{V} \leq SV_{IN} - SV_{OUT}^- \leq 58\text{V}$ , $EXTV_{CC} = \text{Open Circuit}$ $5\text{V} \leq SV_{IN} - SV_{OUT}^- \leq 58\text{V}$ , $3.2\text{V} \leq EXTV_{CC} - V_{OUT}^- \leq 26.5\text{V}$ (INTV <sub>CC</sub> Measured with Respect to $V_{OUT}^-$ )	3.15 2.85	3.4 3.0	3.65 3.15	V V V
$V_{EXTVCC(TH)}$	EXTV <sub>CC</sub> Switchover Voltage	(Note 4)		3.15		V
$\Delta V_{INTVCC(LOAD)}/V_{INTVCC}$	INTV <sub>CC</sub> Load Regulation	$0\text{mA} \leq I_{INTVCC} \leq 30\text{mA}$	-2	0.5	2	%
<b>Temperature Sensor</b>						
$\Delta V_{TEMP}$	Temperature Sensor Forward Voltage, $V_{TEMP}^+ - V_{TEMP}^-$	$I_{TEMP}^+ = 100\mu\text{A}$ and $I_{TEMP}^- = -100\mu\text{A}$ at $T_A = 25^\circ\text{C}$		0.6		V
$TC_{\Delta V(TEMP)}$	$\Delta V_{TEMP}$ Temperature Coefficient			-2.0		mV/°C

**Note 1:** Stresses beyond those listing under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating conditions for extended periods may affect device reliability and lifetime.

**Note 2:** The LTM4651 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTM4651E is guaranteed to meet performance specifications over the  $0^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range. Specifications over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4651I is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** See output current derating curves for different  $V_{IN}$ ,  $V_{OUT}$ , and  $T_A$ , located in the Applications Information section.

**Note 4:** Minimum on-time,  $V_{IN}$  Overvoltage Lockout and Overvoltage Lockout Hysteresis, PGOOD Delay, and EXTV<sub>CC</sub> Switchover Threshold are tested at wafer sort.

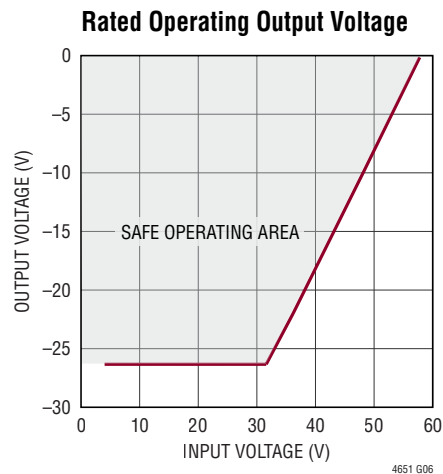
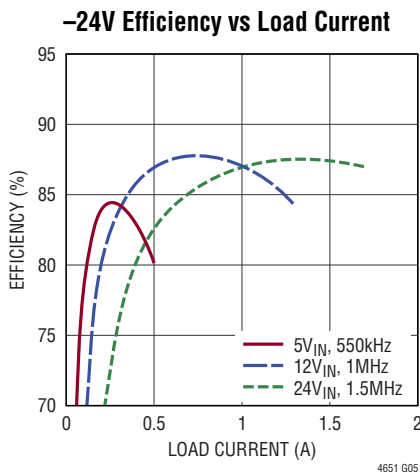
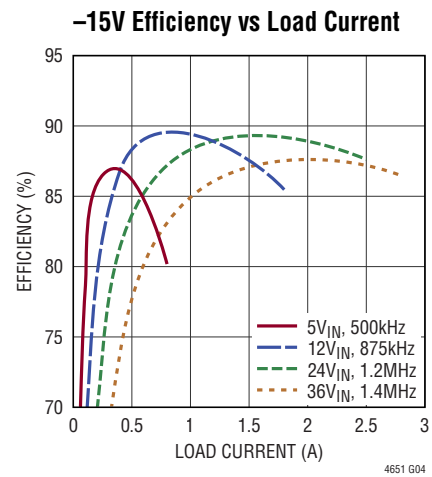
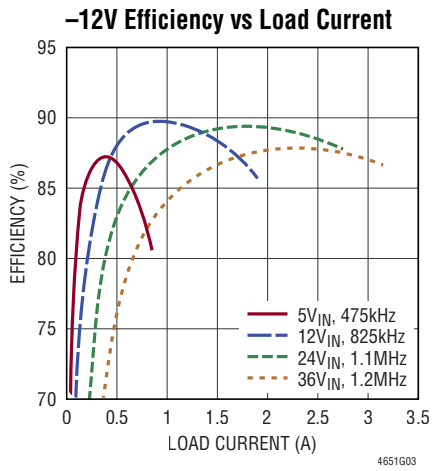
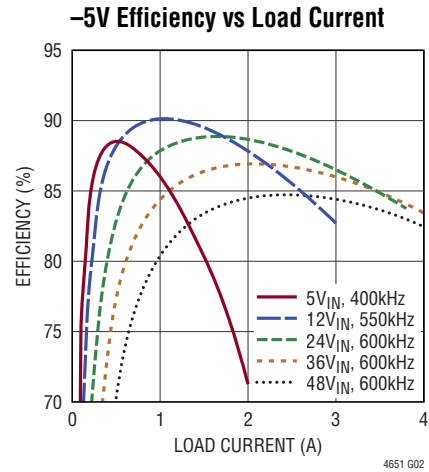
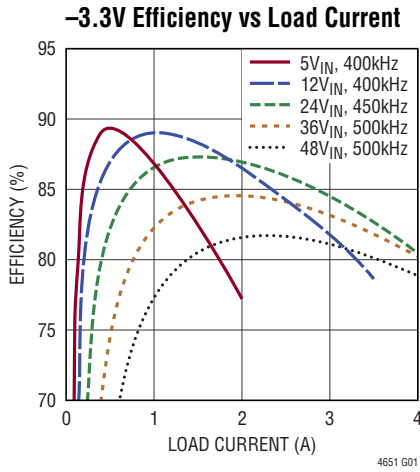
**Note 5:**  $V_{OUT(-0.5VDC)}^-$  low line regulation is tested at  $3.6V_{IN}$ , with  $f_{SET}$  and CLKIN open circuit. High line regulation is tested at  $28V_{IN}$ , and with CLKIN driven at  $200\text{kHz}$ —so as to ensure minimum on time criteria is met. The LTM4651 is not recommended for applications where the minimum on-time criteria (guardband to 90ns) is continuously violated. The LTM4651 can ride through events (such as  $V_{IN}$  surge) where the on-time criteria is transiently violated. See the Applications Information section.

**Note 6:**  $V_{OUT(-24VDC)}^-$  is tested at  $3.6V_{IN}$  and  $34V_{IN}$ , with CLKIN driven with a  $1.8\text{MHz}$  clock,  $ISETa - SV_{OUT}^- = 24\text{V}$ , and  $R_{fSET} = 57.6\text{k}\Omega$ . It is also tested at  $24V_{IN}$ , with CLKIN driven with a  $1.5\text{MHz}$  clock,  $R_{fSET} = 57.6\text{k}\Omega$ , and  $R_{iSET} = 480\text{k}\Omega$ .

**Note 7:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 8:** The INTV<sub>CC</sub> Abs Max peak output current is specified as the sum of current drawn by circuits internal to the module biased off of INTV<sub>CC</sub> and current drawn by external circuits biased off of INTV<sub>CC</sub>. See the Applications Information section.

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



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**-5V Transient Response, 24V<sub>IN</sub>**

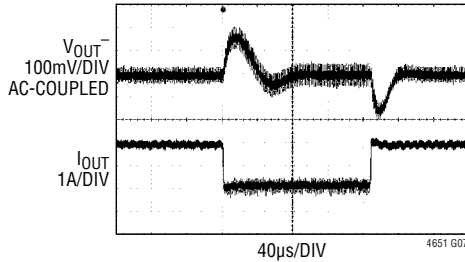


FIGURE 32 CIRCUIT, 24V<sub>IN</sub>,  
 $C_{INOUT} = C_{IN} = C_{DGND} = C_D = 4.7\mu\text{F}$ ,  
 $C_{OUT} = 47\mu\text{F} \times 2$ ,  $R_{ISET} = 665\text{k}\Omega$ ,  
 $R_{ISET} = 100\text{k}\Omega$ ,  $R_{PGDFB} = 36.5\text{k}\Omega$ ,  
 $R_{EXTVCC} = 20\Omega$ , 1.8A TO 3.8A LOAD STEP AT 2A/µs

**-24V Transient Response, 12V<sub>IN</sub>**

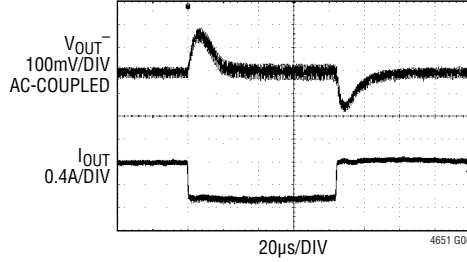


FIGURE 32 CIRCUIT,  
 0.625A TO 1.25A LOAD STEP AT 0.625A/µs

**Start-Up, No Load**

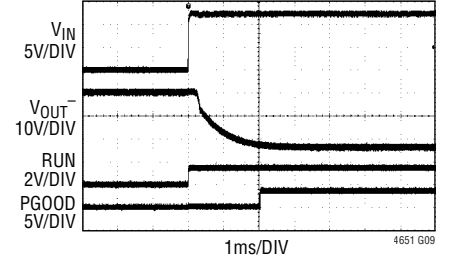


FIGURE 32 CIRCUIT, APPLICATION OF 12V<sub>IN</sub>,  
 START-UP INTO NO LOAD

**Start-Up, 1.25A Load**

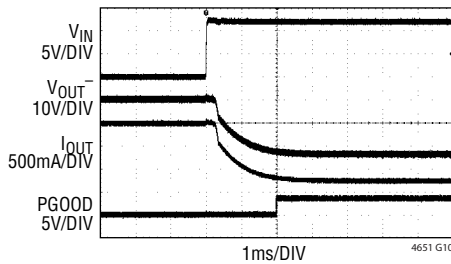


FIGURE 32 CIRCUIT, APPLICATION OF 12V<sub>IN</sub>,  
 START-UP INTO 19.2Ω LOAD

**Start-Up, Pre-Bias**

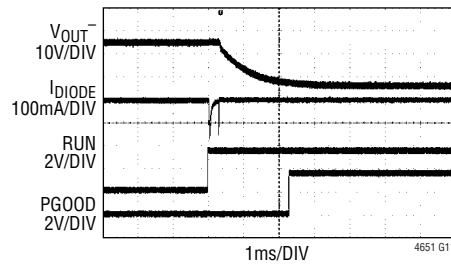


FIGURE 32 CIRCUIT, V<sub>OUT-</sub> PRE-BIASED  
 TO -5V THROUGH A 1N4148 DIODE PRIOR  
 TO RUN TOGGING HIGH

**Short Circuit, No Load**

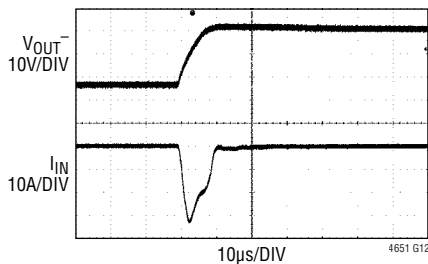


FIGURE 32 CIRCUIT,  
 NO LOAD PRIOR TO APPLICATION OF  
 V<sub>OUT-</sub> SHORT-CIRCUIT

**Short Circuit, 1.25A Load**

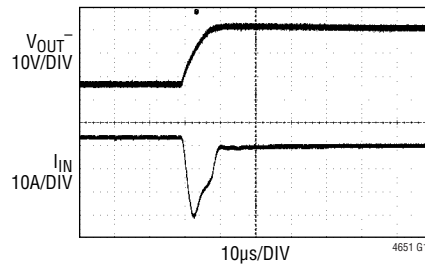


FIGURE 32 CIRCUIT,  
 19.2Ω LOAD PRIOR TO APPLICATION OF  
 V<sub>OUT-</sub> SHORT-CIRCUIT

## PIN FUNCTIONS



**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

**$V_{IN}$  (A1 – A3, B3):** Power Input Pins. Apply input voltage and input decoupling capacitance directly between  $V_{IN}$  and a power ground (PGND) plane.

**$V_D$  (A4, B4, C4):** Drain of the Converter's Primary Switching MOSFET. Apply at least one 4.7 $\mu$ F high frequency ceramic decoupling capacitor directly from  $V_D$  to  $V_{OUT^-}$ . Give this capacitor higher layout priority (closer proximity to the module) than any  $V_{IN}$  decoupling capacitors.

**$SV_{IN}$  (C3):** Input Voltage Supply for Small-Signal Circuits.  $SV_{IN}$  is the input to the INTV<sub>CC</sub> LDO. Connect  $SV_{IN}$  directly to  $V_{IN}$ . No decoupling capacitor is needed on this pin.

**$V_{OUT^-}$  (A5, B5, C2, C5, D5, E5, F5, G4 – 5, H3, H5, J3 – 5, K4 – 5, L4 – 5):** Negative Power Output of the LTM4651. Connect all  $V_{OUT^-}$  pins to the application's  $V_{OUT^-}$  plane. Apply the output filter capacitor and the output load between these and the PGND pins.

**PGND (K1 – 3, L1 – 3):** Power Ground Pins of the LTM4651. Electrically connect all pins to the application's PGND plane.

**GND (D4):** Ground Reference for RUN, CLKIN, and PGOOD Signals. Connect GND directly to the PGND power ground plane.

**$GND_{SNS}$  (G1, H1):** Voltage Sense, PGND Input and Feedback Signal. Connect  $GND_{SNS}$  to PGND at the point of load (POL). Pins G1 and H1 are electronically connected to each other internal to the module, and thus it is only necessary to connect one  $GND_{SNS}$  pin to PGND at the POL. The remaining  $GND_{SNS}$  pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

**$SV_{OUT^-}$  (E4, G2, H2):** Voltage Sense,  $V_{OUT^-}$  Input. Connect Pin H2 to  $V_{OUT^-}$  directly under the LTM4651. The  $SV_{OUT^-}$  pins at locations E4 and G2 are electrically connected to each other internal to the module, and thus it is only necessary to connect one  $SV_{OUT^-}$  pin to  $V_{OUT^-}$  under the module. The remaining  $SV_{OUT^-}$  pins can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

**RUN (F4):** Run Control Pin. A voltage above 1.2V (with respect to GND) commands the module to regulate its output voltage. Undervoltage lockout (UVLO) can be implemented by connecting RUN to the midpoint node formed by a resistor-divider between  $V_{IN}$  and GND. RUN features 130mV of hysteresis. See the Applications Information section.

**INTV<sub>CC</sub> (G3):** Internal Regulator, 3.3V Output with Respect to  $V_{OUT^-}$ . Internal control circuits and MOSFET-drivers derive power from INTV<sub>CC</sub> bias. When operating  $3.6V < SV_{IN} \leq 58V$ , an LDO generates INTV<sub>CC</sub> from  $SV_{IN}$  when RUN is logic high ( $RUN > 1.2V$ ). No external decoupling is required. When RUN is logic low ( $RUN - GND < 1.2V$ ), the INTV<sub>CC</sub> LDO is off, i.e., INTV<sub>CC</sub> is unregulated. (Also see EXT<sub>VCC</sub>.) It is not recommended to load INTV<sub>CC</sub> with external circuits exceeding ~10mA. See the Applications Information section and Note 8.

**EXT<sub>VCC</sub> (F3):** External Bias, Auxiliary Input to the INTV<sub>CC</sub> Regulator. When  $EXTV_{CC} - V_{OUT^-}$  exceeds 3.2V and  $SV_{IN} - V_{OUT^-}$  exceeds 5V, the INTV<sub>CC</sub> LDO derives power from EXT<sub>VCC</sub> bias instead of the  $SV_{IN}$  path. This technique can reduce LDO losses considerably, resulting in a corresponding reduction in module junction temperature. For applications where  $|V_{OUT^-}| > 4V$ , realize this benefit by connecting EXT<sub>VCC</sub> to PGND through a resistor. (See the Application Information section for resistor value.) When taking advantage of this EXT<sub>VCC</sub> feature, locally decouple EXT<sub>VCC</sub> to  $V_{OUT^-}$  with a 1 $\mu$ F ceramic capacitor—otherwise, leave EXT<sub>VCC</sub> open circuit.

**ISETb (F1):** 1.5nF Soft-Start Capacitor. Connect ISETb to ISETa to achieve default soft-start characteristics, if desired—otherwise, leave ISETb open circuit. See ISETa.

**ISETa (F2):** Accurate 50 $\mu$ A Current Source. Positive input to the error amplifier. Connect a resistor ( $R_{SET}$ ) from this pin to  $SV_{OUT^-}$  to program the desired LTM4651 output voltage,  $V_{OUT^-} = -R_{SET} \cdot 50\mu A$ . A capacitor can be connected from ISETa to  $SV_{OUT^-}$  to soft-start the output voltage and reduce start-up inrush current. Connect ISETa to ISETb in order to achieve default soft-start, if desired. See ISETb.



## PIN FUNCTIONS

In addition, the output of the LTM4651 can track a voltage applied between the ISETa pin and the  $SV_{OUT}^-$  pins. See the Applications Information section.

**PGOOD (D1):** Power Good Indicator, Open-Drain Output Pin. PGOOD is high impedance when PGDFB –  $SV_{OUT}^-$  is within approximately  $\pm 7.5\%$  of 0.6V. PGOOD is pulled to GND when PGDFB –  $SV_{OUT}^-$  is outside this range.

**PGDFB (D2):** Power Good Feedback Programming Pin. Connect PGDFB to  $GND_{SNS}$  through a resistor,  $R_{PGDFB}$ .  $R_{PGDFB}$  configures the voltage threshold of  $V_{OUT}^-$  for which PGOOD toggles its state. If the PGOOD feature is used, set  $R_{PGDFB}$  to:

$$R_{PGDFB} = \left( \frac{|V_{OUT}^-|}{0.6V} - 1 \right) \cdot 4.99k$$

otherwise, leave PGDFB open circuit.

A small filter capacitor (220pF) internal to the LTM4651 on this pin provides high frequency noise immunity for the PGOOD output indicator.

**f<sub>SET</sub> (E3):** Oscillator Frequency Programming Pin. The default switching frequency of the LTM4651 is 400kHz. Often, it is necessary to increase the programmed frequency by connecting a resistor between  $f_{SET}$  and  $SV_{OUT}^-$ . (See the Applications Information section.) Note that the synchronization range of CLKIN is approximately  $\pm 40\%$  of the oscillator frequency programmed by the  $f_{SET}$  pin.

**CLKIN (B1):** Oscillator Synchronization Input. Leave CLKIN open circuit for forced continuous mode operation.

Alternatively, this pin can be driven so as to synchronize the switching frequency of the LTM4651 to a clock signal. In this condition, the LTM4651 operates in forced-continuous mode and the cycle-by-cycle turn-on of the Primary MOSFET is coincident with the rising edge of the clock applied to CLKIN. Note the synchronization range of CLKIN is approximately  $\pm 40\%$  of the oscillator frequency programmed by the  $f_{SET}$  pin. See the Applications Information section.

**COMPa (E2):** Current Control Threshold and Error Amplifier Compensation Node. The trip threshold of LTM4651's current comparator increases with a respective rise in COMPa voltage. A small filter capacitor (10pF) internal to the LTM4651 on this pin introduces a high-frequency roll-off of the error-amplifier response, yielding good noise rejection in the control-loop. COMPa is usually electrically connected to COMPb in one's application, thus applying default loop compensation. Loop compensation (a series resistor-capacitor) can be applied externally to COMPa if desired or needed, instead. See COMPb.

**COMPb (E1):** Internal Loop Compensation Network. For a majority of applications, the internal, default loop compensation of the LTM4651 is suitable to apply "as is" and yields very satisfactory results: apply the default loop compensation to the control loop by simply connecting COMPa to COMPb. When more specialized applications require a personal touch to the optimization of control loop response, this can be accomplished by connecting a series resistor-capacitor network from COMPa to  $SV_{OUT}^-$ —and leaving COMPb open circuit.

**VINREG (D3):** Input Voltage Regulation Programming Pin. Optionally connect this pin to the midpoint node formed by a resistor-divider between  $V_D$  and  $SV_{OUT}^-$ . When the voltage on VINREG falls below approximately 2V with respect to  $SV_{OUT}^-$ , a VINREG control loop servos COMPa so as to decrease the power inductor current and thus regulate VINREG at 2V with respect to  $SV_{OUT}^-$ . See the Applications Information section.

If this input voltage regulation feature is not desired, connect VINREG to  $INTV_{CC}$ .

**TEMP<sup>+</sup> (J1, J6):** Temperature Sensor, Positive Input. Emitter of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC<sup>®</sup>2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open. Pins J1 and J6 are electrically connected together internal to the LTM4651, and thus it is only necessary to connect one TEMP<sup>+</sup> pin to monitoring circuitry. The remaining TEMP<sup>+</sup> pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

## PIN FUNCTIONS

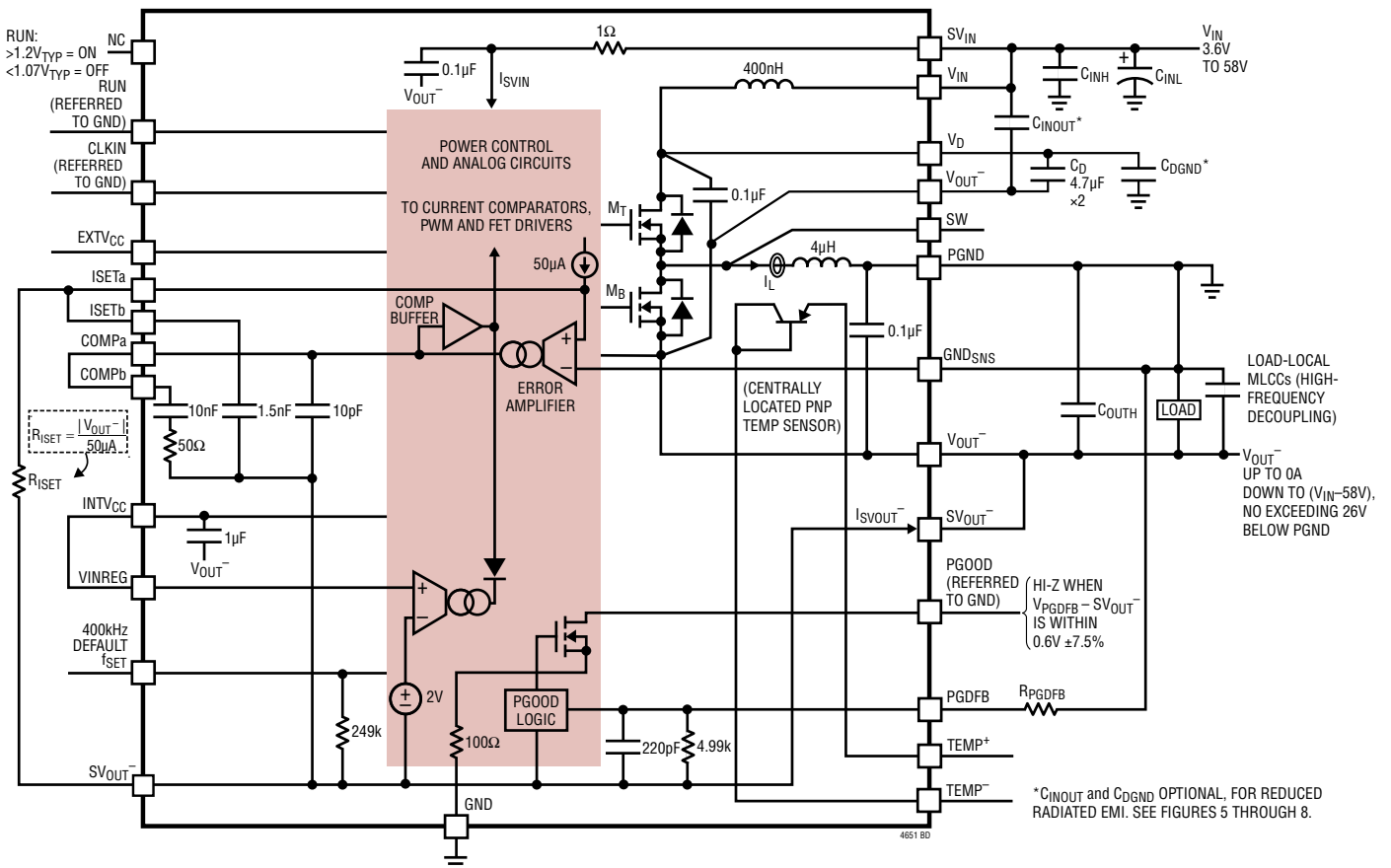
**TEMP<sup>-</sup> (J2, J7):** Temperature Sensor, Negative Input. Collector and base of a 2N3906-genre PNP bipolar junction transistor (BJT). Optionally interface to temperature monitoring circuitry such as LTC2997, LTC2990, LTC2974 or LTC2975. Otherwise leave electrically open. Pins J2 and J7 are electrically connected together internal to the LTM4651, and thus it is only necessary to connect one TEMP<sup>-</sup> pin to monitoring circuitry. The remaining TEMP<sup>-</sup> pin can be used for redundant connectivity or routed to an ICT test point for design-for-test considerations, as desired.

**SW (H4):** Switching Node of Switching Converter Stage. Used for test purposes. May be routed a short distance

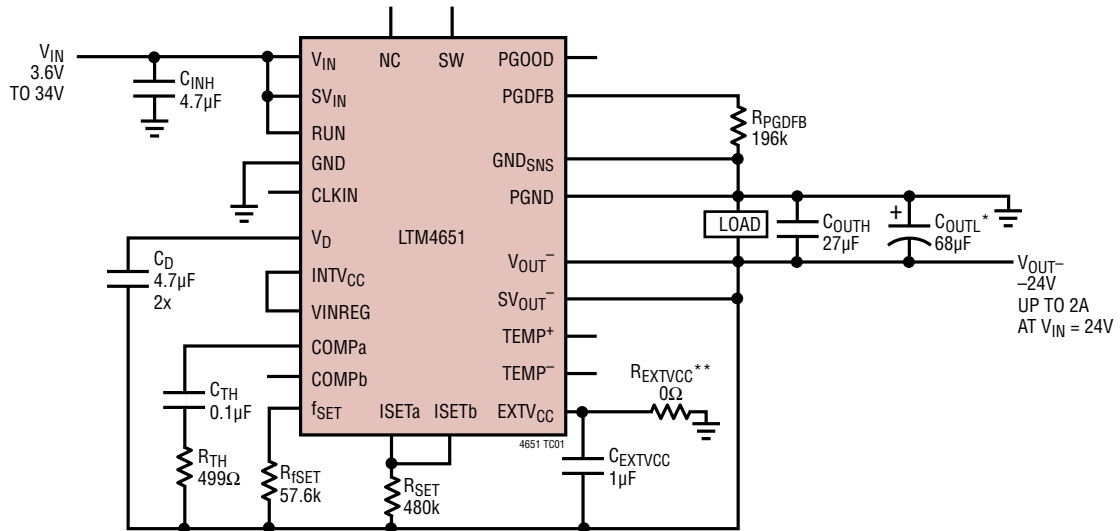
with a thin trace to a local test point to monitor switching action of the converter, if desired, but do not route near any sensitive signals; otherwise, leave electrically open circuit.

**NC (A6 – 7, B2, B6 – 7, C1, C6 – 7, D6 – 7, E6 – 7, F6 – 7, G6 – 7, H6 – 7, K6 – 7, L6 – 7):** No Connect Pins, i.e., Pins with No Internal Connection. The NC pins predominantly serve to provide improved mounting of the module to the board. In one's layout, NC pins are permitted to remain electrically unconnected or can be connected as desired, e.g., connected to a V<sub>OUT<sup>-</sup></sub> plane for heat-spreading purposes and/or to facilitate routing.

## SIMPLIFIED BLOCK DIAGRAM



## TEST CIRCUIT



\*Polarized output capacitors  $C_{OUTL}$ , if used, must be rated to withstand  $\sim 0.3V$  typical reverse polarity prior to LTM4651 start-up, stemming from a weakly forward-biased body diode. In such cases, a Schottky diode should be connected between PGND and  $V_{OUT-}$  to limit the voltage. See the Applications Information section and Figures 33a and 33b.

\*\*Outside the ATE Test environment,  $R_{EXTVCC}$ , if used, should not be  $0\Omega$ . See the Applications Information section.

## DECOUPLING REQUIREMENTS $T_A = 25^\circ C$ . Refer to Test Circuit 1.

APPLICATION	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Test Circuit 1	$C_{INH}, C_D$	External High Frequency Input Capacitor Requirement, $24V \leq V_{IN} \leq 34V, V_{OUT-} = -24V$	2A		9.4		$\mu F$
	$C_{OUTH}$	External High Frequency Output Capacitor Requirement $24V \leq V_{IN} \leq 34V, V_{OUT-} = -24V$	2A		22		$\mu F$

## OPERATION

### Power Module Description

The LTM4651 is a non-isolated switch mode DC/DC power supply. It can provide up to 4A output current with a few external input and output capacitors. Set by a single resistor,  $R_{SET}$ , the LTM4651 regulates a negative output voltage,  $V_{OUT^-}$ .  $V_{OUT^-}$  can be set to as low as  $-26.5V$  to as high as  $-0.5V$ . The LTM4651 operates from a positive input supply rail,  $V_{IN}$ , between  $3.6V$  and  $58V$ . The LTM4651's safe operating area is defined by:  $V_{IN} + |V_{OUT^-}| \leq 58V$ . The typical application schematic is shown in Figure 32. The output current capability of the LTM4651 is dependent on  $V_{IN}$  and  $V_{OUT^-}$ , as indicated in the page 1 graph. Though the LTM4651 is a ground-referred buck converter topology—also known as a two-switch buck-boost converter—it contains built-in level-shift circuitry so that the RUN, CLKIN, and PGOOD pins are conveniently referred to GND (not  $V_{OUT^-}$ ).

The LTM4651 contains an integrated constant-frequency current mode regulator, power MOSFETs, power inductor, EMI filter and other supporting discrete components. The nominal switching frequency range is from  $400kHz$  to  $3MHz$ , and the default operating frequency is  $400kHz$ . It can be externally synchronized to a clock, from  $250kHz$  to  $3MHz$ . See the Applications Information section.

The LTM4651 supports internal and external control loop compensation. Internal loop compensation is selected by connecting the COMPa and COMPb pins. Using internal loop compensation, the LTM4651 has sufficient stability

margins and good transient performance with a wide range of output capacitors, even ceramic-only output capacitors. For external loop compensation, see the Applications Information section. LTpowerCAD® is available for transient load step and stability analysis.

Input filter and noise cancellation circuitry reduces noise-coupling to the module's inputs and outputs, ensuring the module's electromagnetic interference (EMI) meets the limits of EN55022 Class B (see Figures 5 to 8).

Pulling the RUN pin below  $1.2V$  forces the LTM4651 into a shutdown state. A capacitor can be applied from ISETa to  $SV_{OUT^-}$  to program the output voltage ramp-rate; or, the default LTM4651 ramp-rate can be set by connecting ISETa to ISETb; or, voltage tracking can be implemented by interfacing rail voltages to the ISETa pin. See the Application Information section.

Multiphase operation can be employed by applying an external clock source to the LTM4651's synchronization input, the CLKIN pin. See the Typical Applications section.

LDO losses within the module are reduced by connecting  $EXTV_{CC}$  to PGND through an RC-filter or by connecting  $EXTV_{CC}$  to a suitable voltage source.

The LTM4651 also features a spare control pin called VINREG which can be used to reduce the input current draw during input line sag ("brownout") conditions. Connect VINREG to  $INTV_{CC}$  when this feature is not needed.

## APPLICATIONS INFORMATION

The typical LTM4651 application circuit is shown in Test Circuit 1. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 8 for recommended external component values.

### Output Current Capability Varies as a Function of $V_{IN}$ to $V_{OUT}^-$ Conversion Ratios

The output current capability of the LTM4651 has a strong dependency on the operating input ( $V_{IN}$ ) and output ( $V_{OUT}^-$ ) voltages, as highlighted in the page 1 graph.

The reason for this is inherent in the two-switch buck-boost topology employed by the LTM4651. To protect the primary power MOSFET ( $M_T$ ) from overstress (see Simplified Block Diagram), its peak current ( $I_{PK}$ ) is limited by control circuitry to 6A. When  $M_T$  is on, observe that no current flows to LTM4651's output; furthermore, observe that only when  $M_T$  is off does current flow to the output of the LTM4651. As a consequence of this arrangement: for a given output voltage, current limit inception activates sooner at low line (higher, larger duty cycle) than at high line (lower, smaller duty cycle). A further consequence is: for a given input voltage, the output power capability of the LTM4651 is higher for lower-magnitude  $V_{OUT}^-$  (lower, smaller duty cycle) than for higher-magnitude  $V_{OUT}^-$  (higher, larger duty cycle). The combination of these effects is shown the plots in the page 1 graph and described by the following equation:

$$I_{OUT(CAPABILITY)} = \frac{V_{IN} \cdot \left( I_{PK} - \frac{\Delta I_{PK-PK}}{2} \right) \cdot \eta}{V_{IN} - V_{OUT}^-} \quad (1)$$

where:

$\Delta I_{PK-PK}$  is the inductor ripple current, in amps, and  $\eta$  (unitless) is the efficiency of the LTM4651.

For completeness,  $\Delta I_{PK-PK}$  is given by:

$$\Delta I_{PK-PK} = \frac{1}{L \cdot f_{SW} \cdot \left( \frac{1}{V_{IN}} - \frac{1}{V_{OUT}^-} \right)} \quad (2)$$

where:

$L$  is 4 $\mu$ H, the LTM4651's power inductor value, and  $f_{SW}$  is the switching frequency of the LTM4651, in MHz.

For a practical design,  $\Delta I_{PK-PK}$  is designed to be less than  $\sim 2A_{PK-PK}$ .

For a practical design, the LTM4651's on-time of  $M_T$  each switching cycle should be designed to exceed the LTM4651 control loop's specified minimum on-time of 60ns,  $t_{ON(MIN)}$ , (guardband to 90ns) i.e.:

$$\frac{D}{f_{SW}} > T_{ON(MIN)} \quad (3)$$

where  $D$  (unitless) is the duty-cycle of  $M_T$ , given by:

$$D = \frac{-V_{OUT}^-}{V_{IN} - V_{OUT}^-} \quad (4)$$

Combining EQ. 4 with EQ. 1, it can be illustrative to see:

$$I_{OUT(CAPABILITY)} = (1-D) \cdot \left( I_{PK} - \frac{\Delta I_{PK-PK}}{2} \right) \cdot \eta \quad (5)$$

In rare cases where the minimum on-time restriction is violated, the frequency of the LTM4651 automatically and gradually folds back down to one-fifth of its programmed switching frequency to allow  $V_{OUT}^-$  to remain in regulation.

Be reminded of Notes 2, 3 and 5 in the Electrical Characteristics section regarding output current guidelines.

## APPLICATIONS INFORMATION

### Input Capacitors

The LTM4651 achieves low input conducted EMI noise due to tight layout and high-frequency bypassing of MOSFETs  $M_T$  and  $M_B$  within the module itself. A small filter inductor (400nH) is integrated in the input line (from  $V_{IN}$  to  $V_D$ ) provides further noise attenuation—again, local to the switching MOSFETs. The  $V_D$  and  $V_{IN}$  pins are available for external input capacitors— $V_D$  and  $V_{INH}$ —to form a high-frequency  $\pi$  filter. As shown in the Simplified Block Diagram, the ceramic capacitor  $C_D$  on the LTM4651's  $V_D$  pins handles the majority of the RMS current into the DC/DC converter power stage and requires careful selection, for that reason.

To meet the radiated emissions requirements of EN55022B, an additional filter capacitor,  $C_{INOUT}$ , is needed—connecting from  $V_{IN}$  to  $V_{OUT^-}$ . See Figures 5 to 8 for EMI performance.

The input capacitance,  $C_D$ , is needed to filter the pulsed current drawn by  $M_T$ . To prevent excessive voltage sag on  $V_D$ , a low-effective series resistance (low-ESR) input capacitor should be used, sized appropriately for the maximum  $C_D$  RMS ripple current:

$$I_{CD(RMS)} = I_{PK} \cdot \sqrt{D \cdot (1-D)} \quad (6)$$

$I_{CD(RMS)}$  is maximum for  $D = 1/2$ . For  $D = 1/2$ ,  $I_{CD(RMS)} = 1/2 \cdot I_{PK}$  or 3A. This simplification of the worst-case condition is commonly used for design purposes because even significant deviations in  $D$  do not offer much relief, in practice. Furthermore: note that ripple current ratings from capacitor manufacturers are often based on 2000 hours of life; therefore, it is advisable to significantly over-design  $C_D$ , and/or choose a capacitor rated at a higher temperature than required. Err on the side of caution and contact the capacitor manufacturer to understand the capacitor vendor's derating methodology.

Several capacitors may be paralleled to meet the application's target size, height, and  $C_D$  RMS ripple current rating. For lower input voltage applications, sufficient bulk input capacitance is needed for  $C_{INL}$  to counteract line sag and transient effects during output load changes. Suggested values for  $C_D$  and  $C_{INH}$  are found in Table 8. Take note that  $C_D$  is connected from  $V_D$  to  $V_{OUT^-}$ , whereas  $C_{INH}$  and  $C_{INL}$  are connected from  $V_{IN}$  to PGND; this is deliberate.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4651's  $V_{IN}$ ,  $SV_{IN}$ , and  $V_D$  pins. A ceramic input capacitor combined with trace or cable inductance forms a high Q (underdamped) tank circuit. If the LTM4651 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

### Output Capacitors

Output capacitors  $C_{OUTH}$  and  $C_{OUTL}$  are applied to  $V_{OUT^-}$  of the LTM4651: sufficient capacitance and low ESR are called for, to meet the output voltage ripple, loop stability, and transient requirements.  $C_{OUTL}$  can be a low ESR tantalum or polymer capacitor.  $C_{OUTH}$  is a ceramic capacitor. The typical output capacitance is 22 $\mu$ F (type X5R material, or better), if ceramic-only output capacitors are used.

For highest reliability designs, polarized output capacitors ( $V_{OUTL}$ ) are not recommended, as there is a possibility of a diode-drop of reverse voltage appearing transiently on  $V_{OUT^-}$  during rapid application of input voltage or when RUN is toggled logic high (see Figures 33). When polarized capacitors are used on  $V_{OUT^-}$ , contact the capacitor vendor to understand what reverse voltage their polarized capacitor can withstand. Be advised, polarized capacitor reverse voltage rating is sometimes temperature-dependent.

Output voltage ripple ( $\Delta V_{OUT(PK-PK)^-}$ ) is governed by charge lost in  $C_{OUTH}$  and  $C_{OUTL}$  while  $M_T$  is on, in addition to the contribution of a resistive drop across the ESR of the output capacitors. This is expressed by:

$$\Delta V_{OUT(PK-PK)^-} \approx \frac{I_{LOAD} \cdot D}{C_{OUT} \cdot f_{SW}} + \frac{I_{LOAD} \cdot ESR}{D} \quad (7)$$

Table 8 shows a matrix of suggested output capacitors optimized for transient step-loads that are 50% of the full load capability for that combination of  $V_{IN}$ ,  $V_{OUT^-}$ , and  $f_{SW}$ . The table optimizes total equivalent ESR and total bulk capacitance to yield the stated transient-load performance. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. The LTpowerCAD design tool is available for transient and stability analysis.

## APPLICATIONS INFORMATION

### Forced Continuous Operation

Leave the CLKIN pin open circuit to command the LTM4651 for forced continuous operation. In this mode, the control loop is allowed to command the inductor peak current to approximately  $-1\text{A}$ , allowing for significant negative average current.

Clocking the CLKIN pin at a frequency within  $\pm 40\%$  of the target switching frequency commanded by the  $f_{\text{SET}}$  pin synchronizes  $M_T$ 's turn-on to the rising edge of the CLKIN pin.

### Output Voltage Programming, Tracking and Soft-Start

The LTM4651 regulates its output voltage,  $V_{\text{OUT}^-}$ , according to the differential voltage present across ISETa and  $SV_{\text{OUT}^-}$ .

In most applications, the output voltage is set by simply connecting a resistor,  $R_{\text{SET}}$ , from ISETa to  $SV_{\text{OUT}^-}$ , according to:

$$R_{\text{SET}} = \frac{-V_{\text{OUT}^-}}{50\mu\text{A}} \quad (8)$$

Since the LTM4651 control loop servos its output voltage according to the voltage between ISETa and  $SV_{\text{OUT}^-}$ : placing a capacitor,  $C_{\text{SS}}$ , parallel to  $R_{\text{SET}}$  configures the ramp-up rate of ISETa and thus  $V_{\text{OUT}^-}$ . In the time domain, the output voltage ramp-up after the RUN pin is toggled from low to high ( $t = 0\text{s}$ ) is given by:

$$V_{\text{OUT}^-}(t) = I_{\text{ISETa}} \cdot R_{\text{SET}} \cdot \left( 1 - e^{-\frac{t}{R_{\text{SET}} \cdot C_{\text{SET}}}} \right) \quad (9)$$

The soft-start time,  $t_{\text{SS}}$ , is defined as the time it takes for  $V_{\text{OUT}^-}$  to ramp from 0V to 90% of its final value:

$$T_{\text{SS}} = -R_{\text{SET}} \cdot C_{\text{SET}} \cdot \ln(1 - 0.9) \quad (10)$$

or

$$T_{\text{SS}} = 2.3 \cdot R_{\text{SET}} \cdot C_{\text{SET}} \quad (11)$$

A default value of  $C_{\text{SET}} = 1.5\text{nF}$  can be implemented by connecting ISETa to ISETb. For other ramp-up rates, connect an external  $C_{\text{SET}}$  capacitor parallel to  $R_{\text{SET}}$ .

When starting up into a pre-biased  $V_{\text{OUT}^-}$ , the LTM4651 stays in a sleep mode, keeping  $M_T$  and  $M_B$  off until  $V_{\text{ISETa}}$

equals  $V_{\text{GNDSENS}}$ —after which, the DC/DC converter commences switching action and  $V_{\text{OUT}^-}$  is ramped according to the voltage commanded by ISETa.

Since the LTM4651 control loop servos its  $\text{GND}_{\text{SNS}}$  voltage to match that of ISETa's, the LTM4651's output can be configured to track any voltage applied to ISETa, referenced to  $SV_{\text{OUT}^-}$ .

The LTM4651 can track the mirror-image of a positive rail to generate the negative half of a split-supply, as seen in Figure 37.

### Optional Diodes to Guard Against Overstress

Just prior to output voltage start-up, a mechanism exists whereby a diode-drop of reverse polarity can appear on  $V_{\text{OUT}^-}$ . See the simplified Block Diagram and observe: just prior to output voltage start-up,  $SV_{\text{IN}}$  bias current ( $I_{\text{SVIN}}$ ) flows through the module's control IC, to  $SV_{\text{OUT}^-}$ ; from there, the bias current (now  $I_{\text{SVOUT}^-}$ ) flows into  $V_{\text{OUT}^-}$  and through  $M_B$ 's body diode, to SW. This current (now  $I_L$ ) continues to flow—though the  $4\mu\text{H}$  power inductor—to PGND and ground, closing the control IC bias circuit's path. It is this current through  $M_B$ 's body diode that creates a diode-drop of reverse polarity (positive voltage) on  $V_{\text{OUT}^-}$ , as shown in Figure 33. The voltage excursion is highest when RUN toggles high because that is the instant when  $\text{INTV}_{\text{CC}}$  powers-up, with a corresponding increase in  $I_{\text{SVIN}}/I_{\text{SVOUT}^-}/I_L$  current flow. With higher current flow, the forward voltage drop ( $V_F$ ) of  $M_B$ 's body diode—and thus, the positive voltage excursion on  $V_{\text{OUT}^-}$ —is higher.

If this transient voltage excursion is unwelcome for the load or polarized output capacitors, minimize it with a low  $V_F$  Schottky diode that straddles  $V_{\text{OUT}^-}$  and PGND (see Figure 32 circuit and Figure 33 performance). Additionally, the voltage excursion can be empirically reduced by increasing output capacitance.

Lastly: in applications where it is anticipated that  $V_{\text{IN}}$  may be rapidly applied (e.g.,  $<10\mu\text{s}$ ) and  $C_{\text{INOUT}}$  is used, the resulting capacitor-divider network formed by  $C_{\text{INOUT}}$  and  $C_{\text{INL}}||C_{\text{INH}}$  may transiently drag  $V_{\text{OUT}^-}$  positive. It is recommended to apply a low  $V_F$  Schottky diode from  $V_{\text{OUT}^-}$  to PGND, in such applications. The reverse mechanism applies, as well: in applications where it is anticipated that

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$V_{IN}$  may be rapidly discharged and  $C_{INOUT}$  is used, the resulting capacitor-divider network formed by  $C_{INOUT}$  and  $C_{INL}||C_{INH}$  may transiently drag  $V_{OUT-}$  excessively negative. It is recommended to straddle  $V_{OUT-}$  and PGND with a TVS diode, if output voltage excursions during  $V_{IN}$ -discharge are anticipated.

### Frequency Adjustment

The default switching frequency ( $f_{SW}$ ) of the LTM4651 is 400kHz. This is suitable for mainly low- $V_{IN}$  or low- $V_{OUT-}$  applications ( $V_{IN} < 5V$  or  $|V_{OUT-}| < 5V$ ). For a practical design, the LTM4651's inductor ripple current ( $\Delta I_{PK-PK}$ ) is suggested to be less than  $\sim 2A_{PK-PK}$ . From EQ. 2, it follows that  $f_{SW}$  should be chosen such that:

$$f_{SW} = \frac{1}{L \cdot \Delta I_{PK-PK} \cdot \left( \frac{1}{V_{IN}} - \frac{1}{V_{OUT-}} \right)} \quad (12)$$

In some cases, the value of  $f_{SW}$  yielded by EQ. 12 violates the supported minimum on time of the LTM4651 (see EQ. 3). If this occurs, choose  $f_{SW}$  instead according to:

$$f_{SW} < \frac{D}{T_{ON(MIN)}} \quad (13)$$

The primary consequence of using a lower switching frequency than that dictated by EQ. 12 is that the output

current capability of the LTM4651 is reduced, according to EQ. 5.

To configure the LTM4651 for a higher switching frequency than 400kHz default, apply a resistor,  $R_{fSET}$ , between the  $f_{SET}$  pin and  $SV_{OUT-}$ .  $R_{fSET}$  is given (in  $M\Omega$ ) by:

$$R_{fSET} (M\Omega) = \frac{1}{10pF \cdot [f_{SW} (MHz) - 0.4(MHz)]} \quad (14)$$

The relationship of  $R_{fSET}$  to programmed  $f_{SW}$  is shown in Figure 2.

See Table 1 and Table 8 for Recommended  $f_{SW}$  and associated  $R_{fSET}$  values for various combinations of  $V_{IN}$  and  $V_{OUT-}$ .

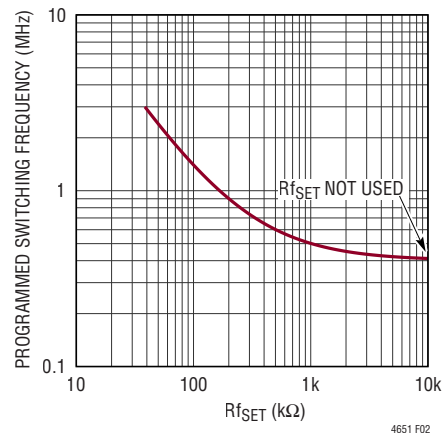


Figure 2. Relationship Between  $R_{fSET}$  and Target  $f_{SW}$

Table 1. Recommended Switching Frequency ( $f_{SW}$ ) and  $R_{fSET}$  Values for Common Combinations of  $V_{IN}$  and  $V_{OUT-}$

		$V_{OUT-}$ (V)							
		-0.5	-3.3	-5	-8	-12	-15	-20	-24
$V_{IN}$ (V)	3.6	400kHz, No $R_{fSET}$	400kHz, No $R_{fSET}$	400kHz, No $R_{fSET}$	400kHz, No $R_{fSET}$	400kHz, No $R_{fSET}$	400kHz, No $R_{fSET}$	425kHz, 4.3M $\Omega$	450kHz, 2.2M $\Omega$
	5				450kHz, 2.2M $\Omega$	475kHz, 1.3M $\Omega$	500kHz, 1M $\Omega$	525kHz, 806k $\Omega$	550kHz, 665k $\Omega$
	12			550kHz, 665k $\Omega$	700kHz, 332k $\Omega$	825kHz, 237k $\Omega$	875kHz, 210k $\Omega$	900kHz, 200k $\Omega$	1MHz, 165k $\Omega$
	24	Drive CLKIN with a 200kHz Clock, No $R_{fSET}$	450kHz, 2.2M $\Omega$	600kHz, 499k $\Omega$	800kHz, 249k $\Omega$	1.1MHz, 143k $\Omega$	1.2MHz, 124k $\Omega$	1.4MHz, 100k $\Omega$	1.5MHz, 90.9k $\Omega$
	36	Not Recommended Due to On- Time Criteria Violation	500kHz, 1M $\Omega$		850kHz, 221k $\Omega$	1.2MHz, 124k $\Omega$	1.4MHz, 100k $\Omega$	1.6MHz, 82.5k $\Omega$	N/A
	48				900kHz, 200k $\Omega$	N/A Due to SOA Criteria Violation			



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### Power Module Protection

The LTM4651's current mode control architecture provides fast cycle-by-cycle current limit in an overcurrent condition, as shown in the Typical Performance Characteristics section. If the output voltage collapses sufficiently due to an overload or short-circuit condition, minimum on-time will be violated (EQ. 3) and the internal oscillator will then fold-back automatically to one-fifth of the LTM4651's programmed switching frequency—hereby reducing the output current and affording the load a chance to recover.

The LTM4651 features input overvoltage shutdown protection: when  $V_{IN} + |V_{OUT}^-| > 68V$ , switching action ceases (with 4V of hysteresis)—however, be advised that this protection is only active outside the LTM4651's safe operating area (see Note 1 and Note 4 of the Electrical Characteristics table).

The LTM4651 ceases switching action if internal temperatures exceed 165°C. The control IC resumes operation after a 10°C cool-down hysteresis. Note that these typical parameters are based on measurements in a lab oven and are not production tested. This overtemperature protection is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

The LTM4651 does not feature any specialized output overvoltage protection beyond what is inherent to the control loop's servo mechanism.

### RUN Pin Enable

The RUN pin is used to enable the power module or sequence the power module. The threshold is 1.2V. The RUN pin can be used to provide an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin, as shown in Figure 3. Undervoltage lockout keeps the LTM4651 in shutdown until the supply input voltage is above a certain voltage programmed by

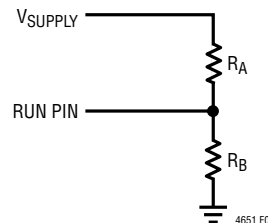


Figure 3. Undervoltage Lockout Resistive Divider

the user. The RUN pin hysteresis voltage prevents noise from falsely tripping UVLO. Resistors are chosen by first selecting  $R_B$  (refer to Figure 3). Then:

$$R_A = R_B \cdot \left( \frac{V_{IN(ON)}}{1.2V} - 1 \right) \quad (15)$$

where  $V_{IN(ON)}$  is the input voltage at which the undervoltage lockout is overcome and the supply turns on.  $R_A$  may be replaced with a hardwired connection from  $V_D$  to RUN. The  $V_{IN}$  turn-off voltage,  $V_{IN(OFF)}$  is given by:

$$V_{IN(OFF)} = 1.07V \cdot \left( \frac{R_A}{R_B} + 1 \right) \quad (16)$$

If UVLO is not needed, RUN can be connected to LTM4651's  $V_D$  or  $V_{IN}$  pins.

When RUN is below its threshold, UVLO is engaged,  $M_T$  and  $M_B$  are turned off,  $INTV_{CC}$  ceases to be regulated, and ISETa is discharged to  $SV_{OUT}^-$  by internal circuitry.

### Loop Compensation

External loop compensation may be preferred for some applications and can be implemented easily, as follows: leave COMPb open circuit; connect a series- $R_C$  network ( $R_{TH}$  and  $C_{TH}$ ) from COMPa to  $SV_{OUT}^-$ ; in some instances, connect a capacitor ( $C_{THP}$ ) from COMPa to  $SV_{OUT}^-$  (paralleling the  $R_{TH}$ - $C_{TH}$  series- $R_C$  network). See Table 8 for suggested input and output capacitances for a variety of operating conditions. Additionally, the LTpowerCAD design tool is available for transient and stability analysis.

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### Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitors ( $C_D$  and  $C_{INH}$ ) of the LTM4651. However, these capacitors can cause problems if the LTM4651 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an under damped tank circuit, and the voltage at the  $V_{IN}$  pin of the LTM4651 can ring to twice the nominal input voltage, possibly exceeding the LTM4651's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM4651 into an energized supply, the input network should be designed to prevent this overshoot by introducing a damping element into the path of current flow. This is often done by adding an inexpensive electrolytic bulk capacitor ( $C_{INL}$ ) across the input terminals of the LTM4651. The selection criteria for  $C_{INL}$  calls for: an ESR high enough to damp the ringing; a capacitance value several times larger than  $C_{INH}$ .  $C_{INL}$  does not need to be located physically close to the LTM4651; it should be located close to the application board's input connector, instead.

### INTV<sub>CC</sub> and EXTV<sub>CC</sub> Connection

When RUN is logic high, an internal low dropout regulator regulates an internal supply, INTV<sub>CC</sub>, that powers the control circuitry for driving LTM4651's internal MOSFETs. INTV<sub>CC</sub> is regulated at 3.3V above  $V_{OUT^-}$ . In this manner, the LTM4651's INTV<sub>CC</sub> is directly powered from  $SV_{IN}$ , by default. The gate driver current through the LDO is about 20mA for a typical 1MHz application. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS(INTVCC)} = 20\text{mA} \cdot (SV_{IN} + |V_{OUT^-}| - 3.3\text{V}) \quad (17)$$

The LDO draws current off of EXTV<sub>CC</sub> instead of  $SV_{IN}$  when EXTV<sub>CC</sub> is tied to a voltage higher than 3.2V above  $V_{OUT^-}$  and  $SV_{IN}$  is 5V above  $V_{OUT^-}$ . For output voltages at or below -4V, this pin can be connected to PGND through an RC-filter. When the internal LDO derives power from EXTV<sub>CC</sub> instead of  $SV_{IN}$ , the internal LDO power dissipation is:

$$P_{LDO\_LOSS(EXTVCC)} = 20\text{mA} \cdot (|V_{OUT^-}| - 3\text{V}) \quad (18)$$

The recommended value of the resistor between PGND and EXTV<sub>CC</sub> is roughly  $|V_{OUT^-}| \cdot 4\Omega/\text{V}$ . This resistor,  $R_{EXTVCC}$ , must be rated to continually dissipate  $(0.02\text{A})^2 \cdot R_{EXTVCC}$ . The primary purpose of this resistor is to prevent EXTV<sub>CC</sub> overstress under a fault condition. For example, when an inductive short-circuit is applied to the module's output,  $V_{OUT^-}$  may be briefly dragged above EXTV<sub>CC</sub>—forward-biasing the  $V_{OUT^-}$ -to-EXTV<sub>CC</sub> body diode. This resistor limits the magnitude of current flow into EXTV<sub>CC</sub>. Bypass EXTV<sub>CC</sub> to  $V_{OUT^-}$  with 1 $\mu\text{F}$  of X5R (or better) MLCC.

### Multiphase Operation

Multiple LTM4651 devices can be paralleled for higher output current applications. For lowest input and output voltage and current ripples, it is advisable to synchronize paralleled LTM4651s to an external clock (within  $\pm 40\%$  of the target switching frequency set by  $f_{SET}$ —see Test Circuit 1). See Figure 34 for an example of a synchronizing circuit.

LTM4651 modules can be paralleled without synchronizing circuits: just be aware that some beat-frequency ripple will be present in the output voltage and reflected input current by virtue of the fact that such modules are not operating at identical, synchronized switching frequencies.

The LTM4651 device is an inherently current mode controlled device, so parallel modules will have good current sharing's shown in Figure 35. This helps balance the thermals on the design.

To parallel LTM4651s, connect the respective COMP<sub>a</sub>, ISET<sub>a</sub>, and GND<sub>SNS</sub> pins of each LTM4651 together to share the current evenly. In addition, tie the respective RUN pins of paralleled LTM4651 devices together, to ensure proper start-up and shutdown behavior. Figure 34 shows a schematic of LTM4651 devices operating in parallel.

Note that for parallel applications, EQ. 8 becomes:

$$R_{SET} = \frac{-V_{OUT^-}}{50\mu\text{A} \cdot N} \quad (19)$$

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where  $N$  is the number of LTM4651 modules in parallel configuration.

Depending on the duty cycle of operation (EQ. 4), the output voltage ripple achieved by paralleled, synchronized LTM4651 modules may be considerably smaller than what is yielded by EQ. 7. Application Note 77 provides a detailed explanation of multiphase operation (relevant to parallel LTM4651 applications) pertaining to noise reduction and output and input ripple current cancellation. Regardless of ripple current cancellation, it remains important for the output capacitance of paralleled LTM4651 applications to be designed for loop stability and transient response. LTpowerCAD is available for such analysis.

Figure 4 illustrates the RMS ripple current reduction as a function of the number of interleaved (paralleled and synchronized) LTM4651 modules—derived from Application Note 77.

### Radiated EMI Noise

The generation of radiated EMI noise is an inherent disadvantage of switching regulators. Fast switching turn-on and turn-off of the power MOSFETs—necessary for achieving high efficiency—create high-frequency ( $\sim 30\text{MHz}+$ )  $\Delta I/\Delta t$  changes within DC/DC converters. This activity tends to be the dominant source of high-frequency EMI radiation in such systems. The high level of device integration within LTM4651—including optimized gate-driver and critical front-end  $\pi$  filter inductor—delivers low radiated EMI noise performance. Figures 5 to 8 show typical examples of LTM4651 meeting the radiated emission limits established by EN55022 Class B.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of this data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a  $\mu$ Module package mounted to a hardware test board.

The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the  $\mu$ Module regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1.  $\theta_{JA}$ , the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2.  $\theta_{Jcbottom}$ , the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical  $\mu$ Module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don’t generally match the user’s application.
3.  $\theta_{Jctop}$ , the thermal resistance from junction to top of the product case, is determined with nearly all of the

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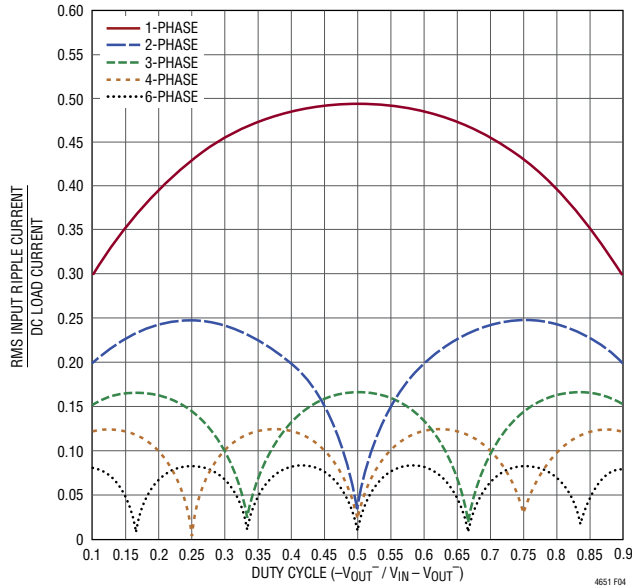


Figure 4. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six LTM4651s (Phases)

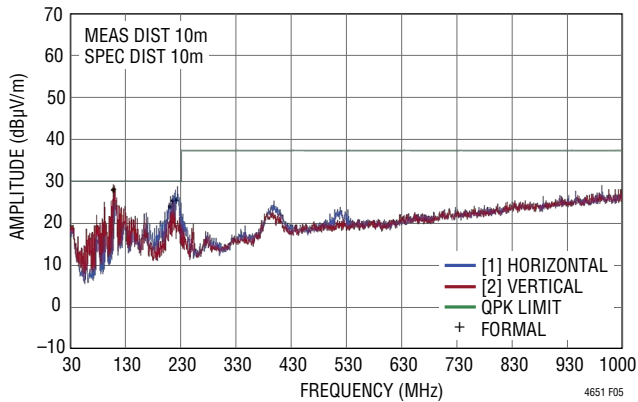


Figure 5. Radiated Emissions Scan of the LTM4651. Producing  $-24V_{OUT}$  at 1A, from  $12V_{IN}$ . DC2328A Hardware.  $f_{SW} = 1.2MHz$ . Measured in a 10m Chamber. Peak Detect Method

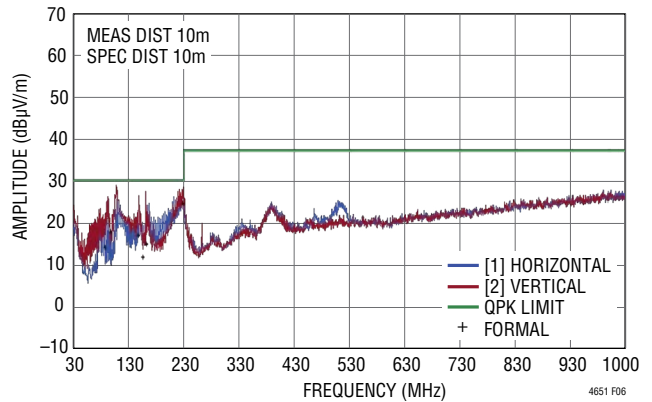


Figure 6. Radiated Emissions Scan of the LTM4651 Producing  $-24V_{OUT}$  at 2A, from  $25V_{IN}$ . DC2328 Hardware.  $f_{SW} = 1.2MHz$ . Measured in a 10m Chamber. Peak Detect Method

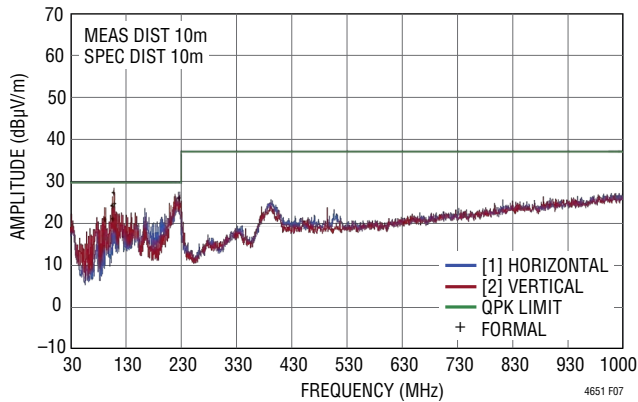


Figure 7. Radiated Emissions Scan of the LTM4651. Producing  $-24V_{OUT}$  at 2A, from  $34V_{IN}$ . DC2328A Hardware.  $f_{SW} = 1.2MHz$ . Measured in a 10m Chamber. Peak Detect Method

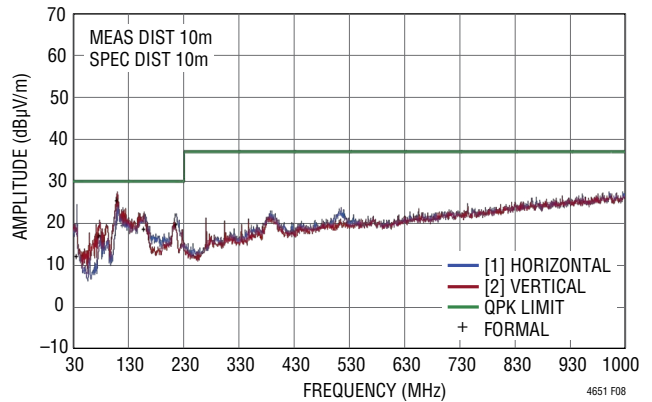


Figure 8. Radiated Emissions Scan of the LTM4651. Producing  $-12V_{OUT}$  at 2A, from  $12V_{IN}$ . DC2328A Hardware.  $f_{SW} = 700kHz$ . Measured in a 10m Chamber. Peak Detect Method

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component power dissipation flowing through the top of the package. As the electrical connections of the typical  $\mu$ Module regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of  $\theta_{JCbottom}$ , this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4.  $\theta_{JB}$ , the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the  $\mu$ Module regulator and into the board, and is really the sum of the  $\theta_{JCbottom}$  and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the  $\mu$ Module regulator, whereas green resistances are external to the  $\mu$ Module package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a  $\mu$ Module regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct

exclusively through the top or exclusively through bottom of the  $\mu$ Module package—as the standard defines for  $\theta_{JCtop}$  and  $\theta_{JCbottom}$ , respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4651, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4651 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 and JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4651 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated

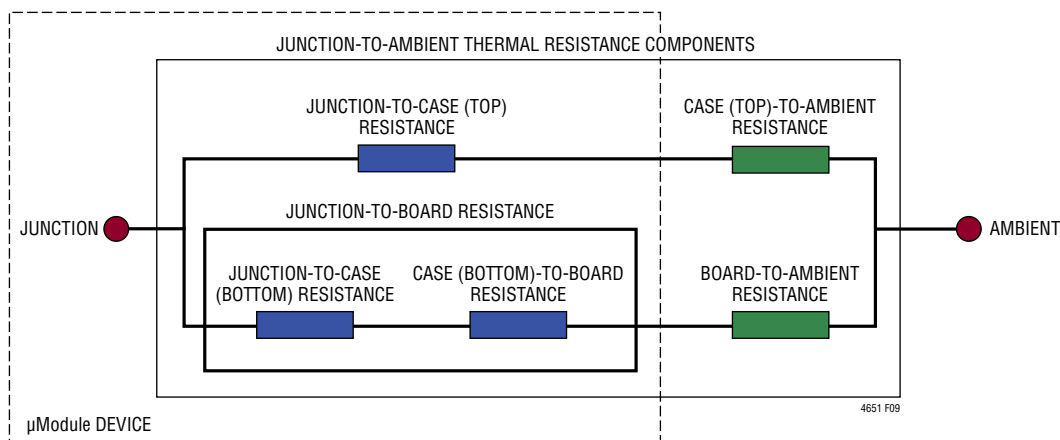


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

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conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JEDEC51-12-defined  $\theta$  values provided in the Pin Configuration section of this data sheet.

The  $-5V$ ,  $-15V$  and  $-24V$  power loss curves in Figures 10, 11 and 12 respectively can be used in coordination with the load current derating curves in Figures 13 to 30 for calculating an approximate  $\theta_{JA}$  thermal resistance for the LTM4651 with various heat sinking and air flow conditions. These thermal resistances represent demonstrated performance of the LTM4651 on DC2328A hardware; a 4-layer FR4 PCB measuring 99mm  $\times$  133mm  $\times$  1.6mm using outer and inner copper weights of 2oz and 1oz, respectively. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are listed in Table 2. (Compute the factor by interpolation, for intermediate temperatures.) The derating curves are plotted with the LTM4651's output initially sourcing its maximum output capability (see Eq. 5) and the ambient temperature at 30°C. The output voltages are  $-5V$ ,  $-15V$  and  $-24V$ . These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. In all derating curves, the switching frequency of operation follows guidance provided by Table 1. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current decreases the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module

temperature rise can be allowed. As an example in Figure 26, the load current is derated to 1A at 60°C ambient with 200LFM airflow and no heat sink and the room temperature (25°C) power loss for this 12V<sub>IN</sub> to  $-24V_{OUT}$  at 1A out condition is 3.55W. A 3.9W loss is calculated by multiplying the 3.55W room temperature loss from the 12V<sub>IN</sub> to  $-24V_{OUT}$  power loss curve at 1A (Figure 12), with the 1.1 multiplying factor at 60°C ambient (from Table 2). If the 60°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 60°C divided by 3.9W yields a thermal resistance,  $\theta_{JA}$ , of 15.4°C/W—in good agreement with Table 4. Tables 3, 4 and 5 provide equivalent thermal resistances for  $-5V$ ,  $-15V$  and  $-24V$  outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 3, 4 and 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with ambient temperature multiplicative factors from Table 2.

**Table 2. Power Loss Multiplicative Factors vs Ambient Temperature**

AMBIENT TEMPERATURE	POWER LOSS MULTIPLICATIVE FACTOR
Up to 40°C	1.00
50°C	1.05
60°C	1.10
70°C	1.15
80°C	1.20
90°C	1.25
100°C	1.30
110°C	1.35
120°C	1.40

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**Table 3. –5V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 13, 14, 15	5, 12, 24	Figure 10	0	None	20.8
Figures 13, 14, 15	5, 12, 24	Figure 10	200	None	17.0
Figures 13, 14, 15	5, 12, 24	Figure 10	400	None	16.3
Figures 16, 17, 18	5, 12, 24	Figure 10	0	BGA Heat Sink	18.7
Figures 16, 17, 18	5, 12, 24	Figure 10	200	BGA Heat Sink	16.1
Figures 16, 17, 18	5, 12, 24	Figure 10	400	BGA Heat Sink	14.2

**Table 4. –15V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 19, 20, 21	5, 12, 24	Figure 11	0	None	20.0
Figures 19, 20, 21	5, 12, 24	Figure 11	200	None	16.6
Figures 19, 20, 21	5, 12, 24	Figure 11	400	None	14.4
Figures 22, 23, 24	5, 12, 24	Figure 11	0	BGA Heat Sink	19.0
Figures 22, 23, 24	5, 12, 24	Figure 11	200	BGA Heat Sink	14.2
Figures 22, 23, 24	5, 12, 24	Figure 11	400	BGA Heat Sink	12.6

**Table 5. –24V Output**

DERATING CURVE	V <sub>IN</sub> (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ <sub>JA</sub> (°C/W)
Figures 25, 26, 27	5, 12, 24	Figure 12	0	None	18.3
Figures 25, 26, 27	5, 12, 24	Figure 12	200	None	15.2
Figures 25, 26, 27	5, 12, 24	Figure 12	400	None	14.4
Figures 28, 29, 30	5, 12, 24	Figure 12	0	BGA Heat Sink	17.6
Figures 28, 29, 30	5, 12, 24	Figure 12	200	BGA Heat Sink	14.7
Figures 28, 29, 30	5, 12, 24	Figure 12	400	BGA Heat Sink	13.9

**Table 6. Heat Sink Manufacturer (Thermally Conductive Adhesive Tape Pre-Attached)**

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Cool Innovations	3-0504035UT411	www.coolinnovations.com

**Table 7. Thermally Conductive Adhesive Tape Vendor**

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chomerics	T411	www.chomerics.com

## APPLICATIONS INFORMATION

**Table 8. LTM4651 Output Voltage Response vs Component Matrix. Performance of Figure 32 Circuit with Values Here Indicated, COMPa Connected to COMb, C<sub>EXTVCC</sub> = 1μF, and the Following Components Not Used: C<sub>TH</sub>, R<sub>TH</sub> and C<sub>OUTL</sub>. Load-Stepping from 50% of Full Scale (F.S.) to 100% of F.S. Load Current, in 1μs. Typical Measured Values**

C <sub>OUTH</sub> VENDORS	PART NUMBER	C <sub>IN</sub> /C <sub>D</sub> VENDORS	PART NUMBER
AVX	12066D107MAT2A (100μF, 6.3V, 1206 Case Size)	Murata	GRM32ER71K475M (4.7μF, 80V, 1210 Case Size)
Murata	GRM31CR60J107M (100μF, 6.3V, 1206 Case Size)	AVX	12065C475MAT2A (4.7μF, 50V, 1206 Case Size)
Taiyo Yuden	JMK316BBJ107MLHT (100μF, 6.3V, 1206 Case Size)	Murata	GRM31CR71H475M (4.7μF, 50V, 1206 Case Size)
TDK	C3216X5R0J107M (100μF, 6.3V, 1206 Case Size)	Taiyo Yuden	UMK316AB7475ML (4.7μF, 50V, 1206 Case Size)
AVX	1210YD476MAT2A (47μF, 16V, 1210 Case Size)	TDK	C3216X5R1H475M (4.7μF, 50V, 1206 Case Size)
Murata	GRM32ER61C476M (47μF, 16V, 1210 Case Size)		
Taiyo Yuden	EMK325BJ476MM (47μF, 16V, 1210 Case Size)		
AVX	12103D226MAT2A (22μF, 25V, 1210 Case Size)		
Taiyo Yuden	TMK325BJ226MM (22μF, 25V, 1210 Case Size)		
TDK	C3225X5R1E226M (22μF, 25V, 1210 Case Size)		
AVX	12105D106MAT2A (10μF, 50V, 1210 Case Size)		
Murata	GRM32ER61H106M (10μF, 50V, 1210 Case Size)		
Taiyo Yuden	UMK325BJ106M (10μF, 50V, 1210 Case Size)		
TDK	C3225X5R1H106M (10μF, 50V, 1210 Case Size)		

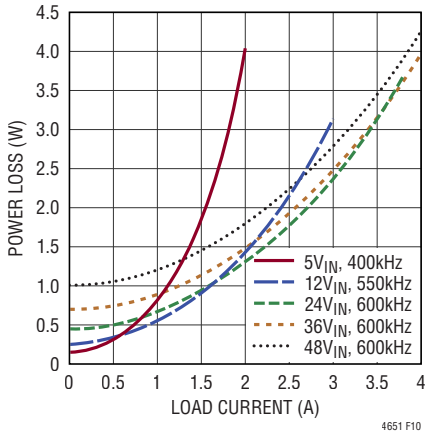
V <sub>OUT-</sub> (V)	V <sub>IN</sub> (V)	F. S. LOAD (A)	C <sub>IN</sub> (V <sub>IN-</sub> TO GND BYPASS CAP)	C <sub>INOUT</sub> (V <sub>IN-</sub> TO V <sub>OUT-</sub> BYPASS CAP)	C <sub>D</sub> (V <sub>D-</sub> TO V <sub>OUT-</sub> BYPASS CAP)	CDGND (V <sub>D-</sub> TO GND BYPASS CAP)	C <sub>OUTH</sub> (CERAMIC OUTPUT CAP)	R <sub>ISSET</sub> (kΩ)	R <sub>PGDFB</sub> (kΩ)	f <sub>sw</sub> (kHz)	R <sub>ISSET</sub> (kΩ)	R <sub>EXTVCC</sub> (Ω)	LOAD STEP TRANSIENT DROOP (mV)	LOAD STEP PK-PK DEVIATION (mV)	RECOVERY TIME (μs)
-0.5	5	3.2	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 4	10	N/A	400	N/A	2.2	75	150	55
-0.5	12	4	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 4	10	N/A	400	N/A	2.2	90	190	60
-0.5*	24	4	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 4	10	N/A	200*	N/A	2.2	90	190	60
-3.3	5	2.2	4.7μF	4.7μF	4.7μF	4.7μF	100μF	66.5	22.6	400	N/A	15	65	130	25
-3.3	12	3.5	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 2	66.5	22.6	400	N/A	15	165	330	50
-3.3	24	4	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 2	66.5	22.6	450	2200	15	175	355	50
-3.3	36	4	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 2	66.5	22.6	500	1000	15	160	310	40
-3.3	48	4	4.7μF	4.7μF	4.7μF	4.7μF	100μF × 2	66.5	22.6	500	1000	15	152	300	35
-5	5	1.75	4.7μF	4.7μF	4.7μF	4.7μF	47μF × 2	100	36.5	400	N/A	20	125	235	45
-5	12	3.2	4.7μF	4.7μF	4.7μF	4.7μF	47μF × 2	100	36.5	550	665	20	175	340	60
-5	24	3.85	4.7μF	4.7μF	4.7μF	4.7μF	47μF × 2	100	36.5	600	499	20	185	380	55
-5	36	4	4.7μF	4.7μF	4.7μF	4.7μF	47μF × 2	100	36.5	600	499	20	180	360	45
-5	48	4	4.7μF	4.7μF	4.7μF	4.7μF	47μF × 2	100	36.5	600	499	20	165	330	38
-8	5	1.2	4.7μF	4.7μF	4.7μF	4.7μF	47μF	160	61.9	450	2200	32.4	125	235	30
-8	12	2.3	4.7μF	4.7μF	4.7μF	4.7μF	47μF	160	61.9	700	332	32.4	185	340	30
-8	24	3.1	4.7μF	4.7μF	4.7μF	4.7μF	47μF	160	61.9	800	249	32.4	180	330	27
-8	36	3.4	4.7μF	4.7μF	4.7μF	4.7μF	47μF	160	61.9	850	221	32.4	205	400	27
-8	48	3.6	4.7μF	4.7μF	4.7μF	4.7μF	47μF	160	61.9	900	200	32.4	185	370	25
-12	5	0.9	4.7μF	4.7μF	4.7μF	4.7μF	22μF	240	95.3	475	1300	49.9	140	270	32
-12	12	1.9	4.7μF	4.7μF	4.7μF	4.7μF	22μF	240	95.3	825	237	49.9	157	290	25
-12	24	2.75	4.7μF	4.7μF	4.7μF	4.7μF	22μF	240	95.3	1100	143	49.9	170	325	25
-12	36	3.2	4.7μF	4.7μF	4.7μF	4.7μF	22μF	240	95.3	1200	124	49.9	200	400	25
-15	5	0.75	4.7μF	4.7μF	4.7μF	4.7μF	22μF	301	121	500	1000	60.4	90	170	25
-15	12	1.75	4.7μF	4.7μF	4.7μF	4.7μF	22μF	301	121	875	210	60.4	200	380	32
-15	24	2.5	4.7μF	4.7μF	4.7μF	4.7μF	22μF	301	121	1200	124	60.4	205	400	28
-15	36	3	4.7μF	4.7μF	4.7μF	4.7μF	22μF	301	121	1400	100	60.4	210	415	28
-24	5	0.55	4.7μF	4.7μF	4.7μF × 2	4.7μF × 2	10μF × 2	481	196	550	665	100	105	220	45
-24	12	1.25	4.7μF	4.7μF	4.7μF × 2	4.7μF × 2	10μF × 2	481	196	1000	165	100	140	275	30
-24	24	2	4.7μF	4.7μF	4.7μF × 2	4.7μF × 2	10μF × 2	481	196	1500	90.9	100	140	280	27

\*To avoid violating minimum on-time criteria, drive CLKIN with a 200kHz, 50% duty cycle clock. Consider using LTC6908-1, for example.

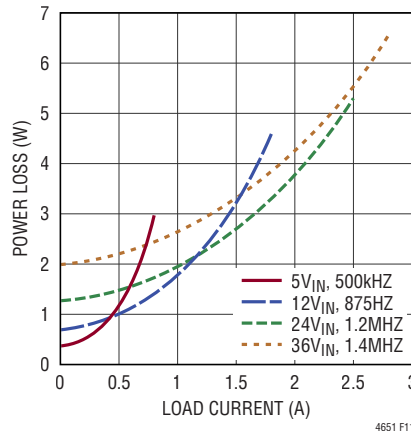


**APPLICATIONS INFORMATION—DERATING CURVES**

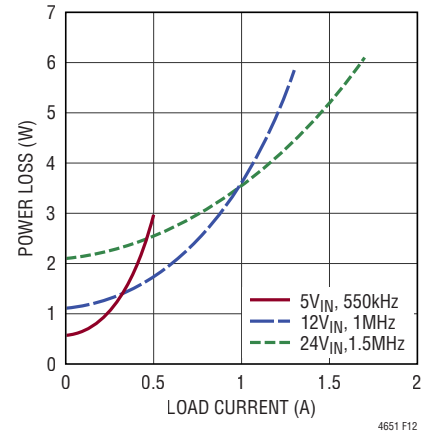
See Table 1 for  $f_{sw}$ .



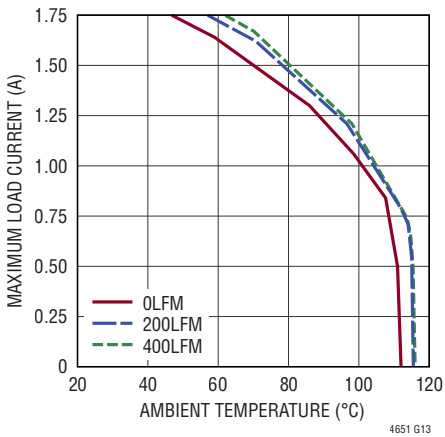
**Figure 10. -5V<sub>OUT</sub> Power Loss Curve**



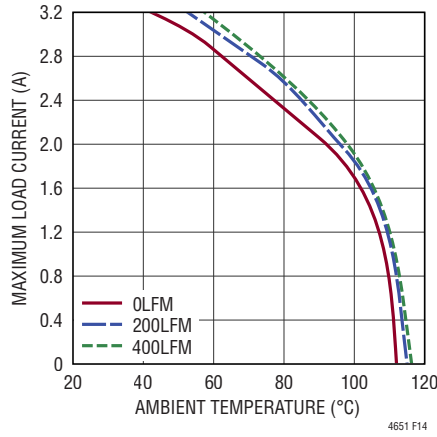
**Figure 11. -15V<sub>OUT</sub> Power Loss Curve**



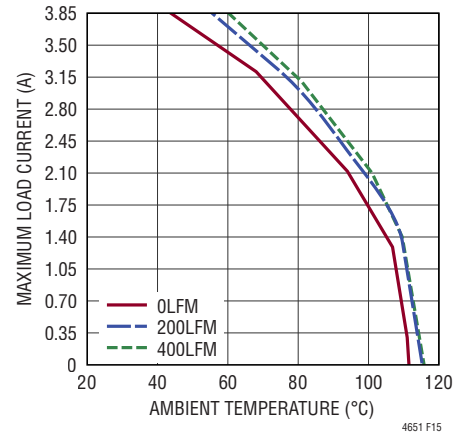
**Figure 12. -24V<sub>OUT</sub> Power Loss Curve**



**Figure 13. 5V to -5V Derating Curve, No Heat Sink**



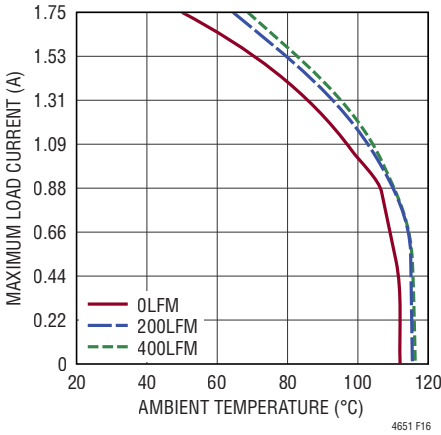
**Figure 14. 12V to -5V Derating Curve, No Heat Sink**



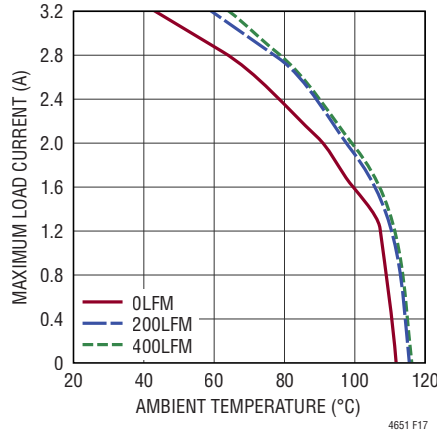
**Figure 15. 24V to -5V Derating Curve, No Heat Sink**

**APPLICATIONS INFORMATION—DERATING CURVES**

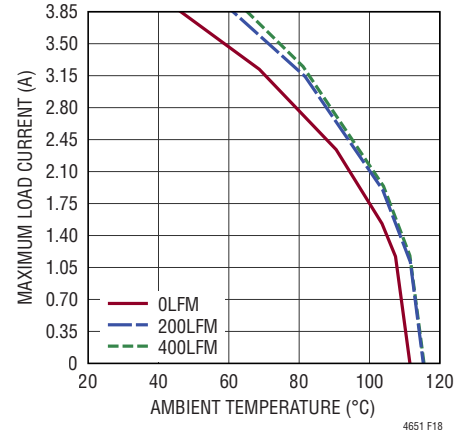
See Table 1 for  $f_{SW}$ .



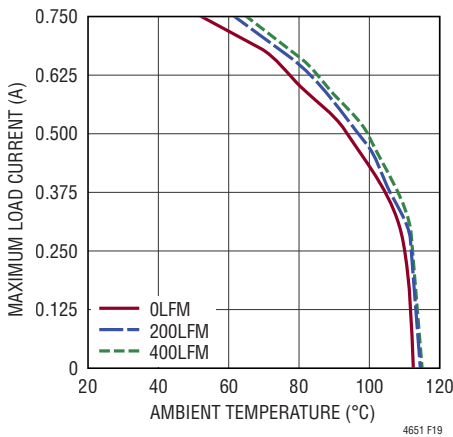
**Figure 16. 5V to -5V Derating Curve, with BGA Heat Sink**



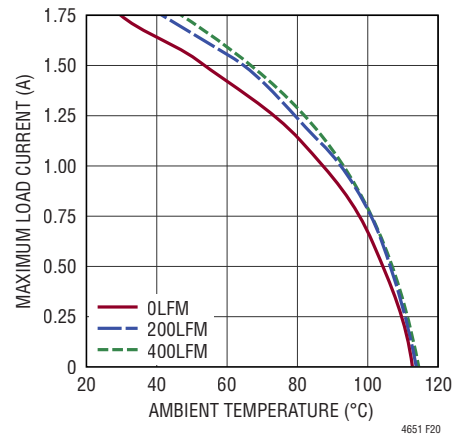
**Figure 17. 12V to -5V Derating Curve, with BGA Heat Sink**



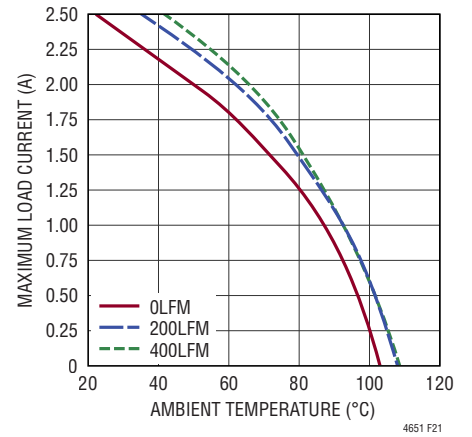
**Figure 18. 24V to -5V Derating Curve, with BGA Heat Sink**



**Figure 19. 5V to -15V Derating Curve, No Heat Sink**



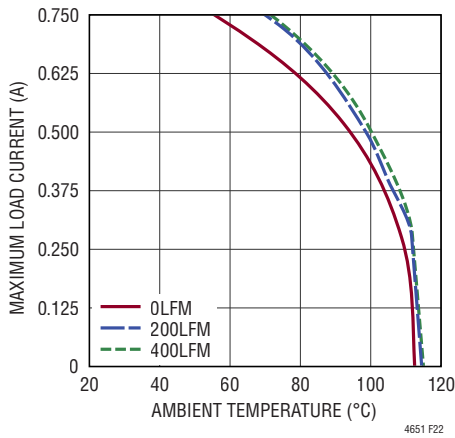
**Figure 20. 12V to -15V Derating Curve, No Heat Sink**



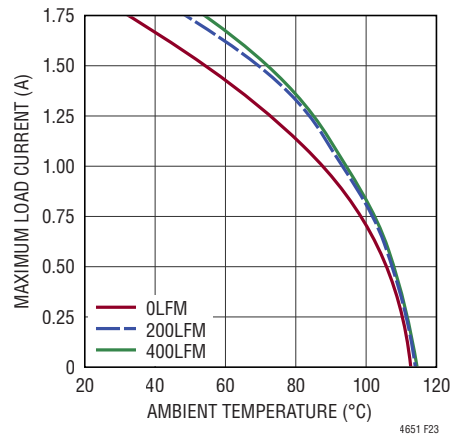
**Figure 21. 24V to -15V Derating Curve, No Heat Sink**

**APPLICATIONS INFORMATION—DERATING CURVES**

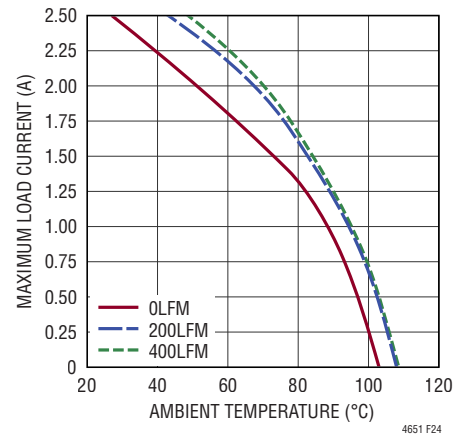
See Table 1 for  $f_{SW}$ .



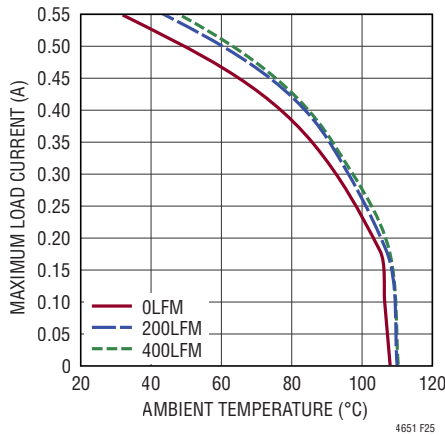
**Figure 22. 5V to -15V Derating Curve, with BGA Heat Sink**



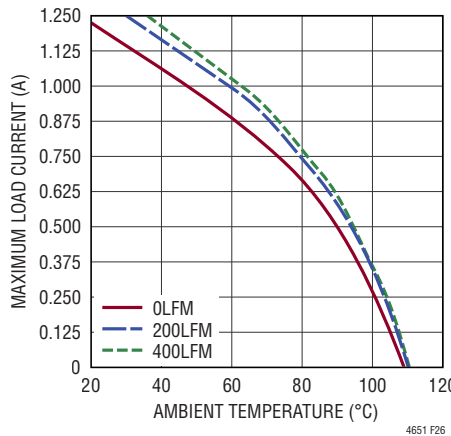
**Figure 23. 12V to -15V Derating Curve, with BGA Heat Sink**



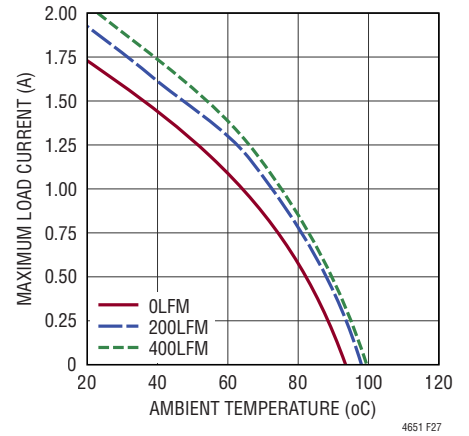
**Figure 24. 24V to -15V Derating Curve, with BGA Heat Sink**



**Figure 25. 5V to -24V Derating Curve, No Heat Sink**



**Figure 26. 12V to -24V Derating Curve, No Heat Sink**



**Figure 27. 24V to -24V Derating Curve, No Heat Sink**

## APPLICATIONS INFORMATION—DERATING CURVES

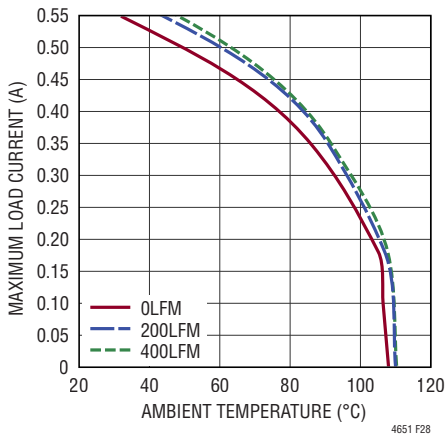


Figure 28. 5V to -24V Derating Curve, with BGA Heat Sink

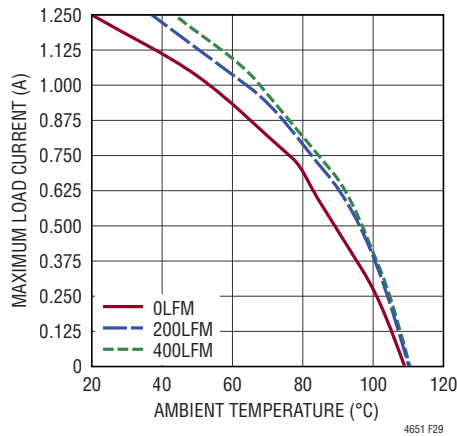


Figure 29. 12V to -24V Derating Curve, with BGA Heat Sink

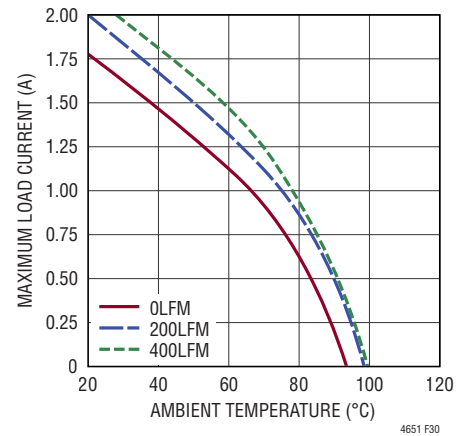


Figure 30. 24V to -24V Derating Curve, with BGA Heat Sink

## APPLICATIONS INFORMATION

### Safety Considerations

The LTM4651 does not provide galvanic isolation from  $V_{IN}$  to  $V_{OUT-}$ . There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect the unit from catastrophic failure.

The fuse or circuit breaker, if used, should be selected to limit the current to the regulator in case of a  $M_T$  MOSFET fault. If  $M_T$  fails, the system's input supply will source very large currents to PGND through  $M_T$ . This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The LTM4651 does feature overcurrent and overtemperature protection.

### Layout Checklist/Example

The high integration of LTM4651 makes the PCB board layout straightforward. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including  $V_{IN}$ , PGND and  $V_{OUT-}$ . Doing so helps to minimize the PCB conduction loss and thermal stress.

- Place high frequency ceramic input and output (and, if used, input-to-output) capacitors next to the  $V_{IN}$ ,  $V_D$ , PGND and  $V_{OUT-}$  pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the LTM4651.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads, unless they are capped or plated over.
- Use a separate  $SV_{OUT-}$  copper plane for components connected to signal pins. Connect  $SV_{OUT-}$  to  $V_{OUT-}$  directly under the module.
- For parallel module applications, connect the  $V_{OUT-}$ ,  $GND_{SNS}$ , RUN, ISETa, COMPa and PGOOD pins together as shown in Figure 41.
- Bring out test points on the signal pins for monitoring.

Figure 31 gives a good example of the recommended LTM4651 layout.

## APPLICATIONS INFORMATION

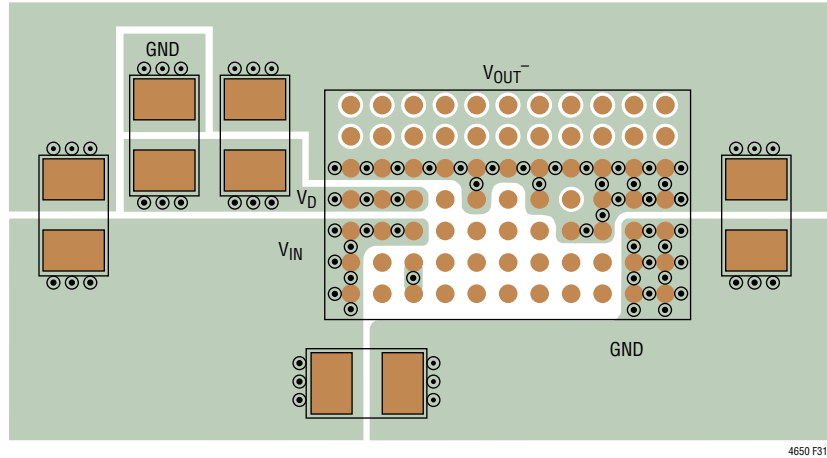
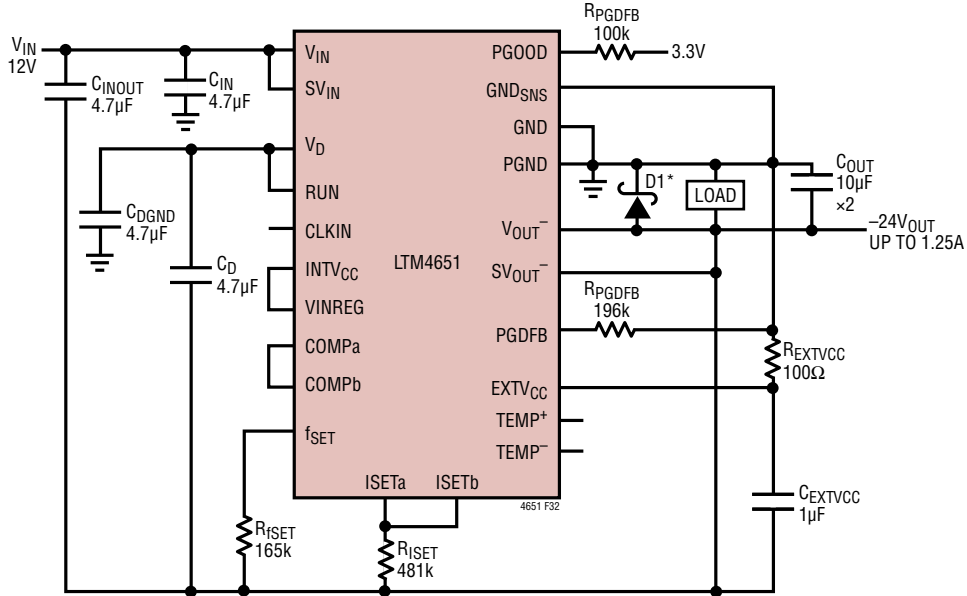


Figure 31. Recommend PCB Layout, Package Top View

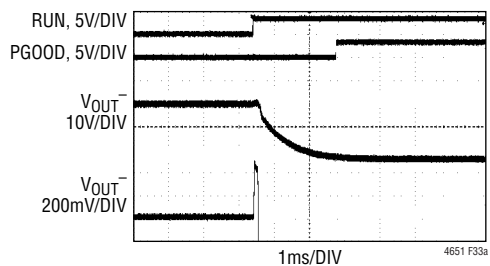
## TYPICAL APPLICATIONS



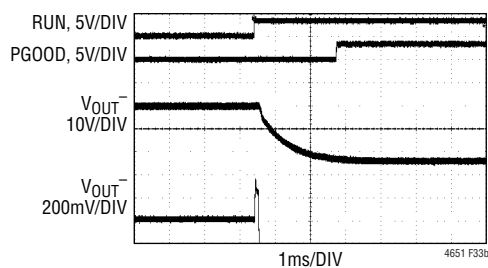
\*D1 optional (see effect in Figure 33): Central Semiconductor P/N CMMSH1-40L

Figure 32. 1.25A, -24V Output DC/DC  $\mu$ Module Regulator

## TYPICAL APPLICATIONS



**(a) Start-up Performance with D1 Not Installed.  
 $V_{OUT-}$  Reverse-Polarity at Start-Up Transiently  
Reaches 500mV**



**(b) Start-up Performance with D1 Installed.  
 $V_{OUT-}$  Reverse-Polarity at Start-Up is Transiently  
Limited to 360mV**

**Figure 33. Start-Up Waveforms at 12V<sub>IN</sub>, Figure 32 Circuit**

TYPICAL APPLICATIONS

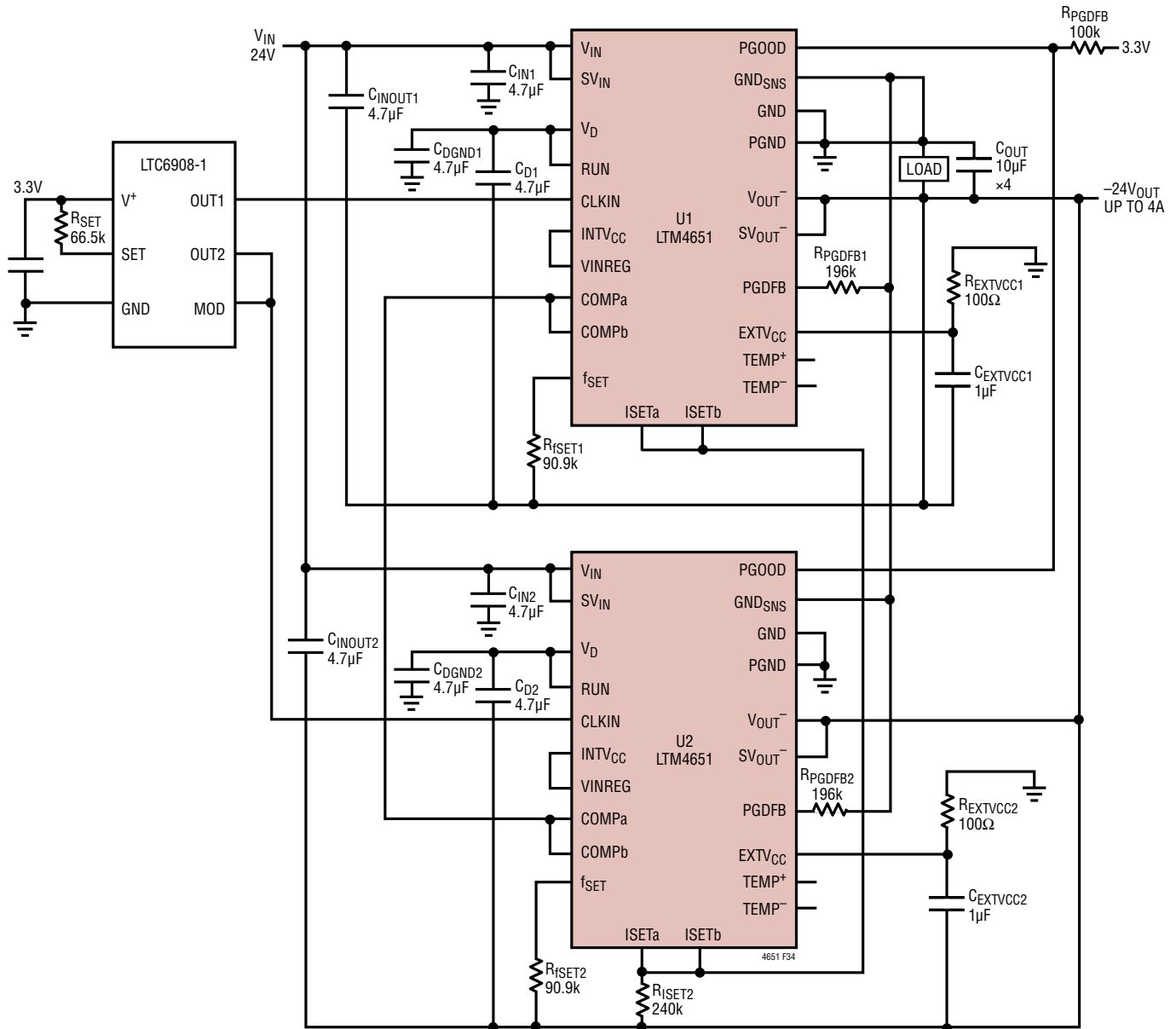


Figure 34. -24V Output at Up to 4A from 24V Input, 2-Phase Interleaved, Parallel Application at  $f_{sw} = 1.5\text{MHz}$

## TYPICAL APPLICATIONS

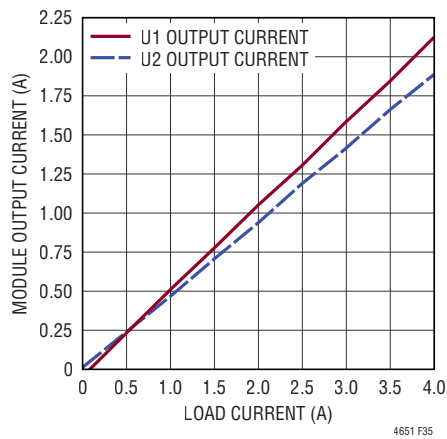


Figure 35. Current Sharing Performance of LTM4651s in Figure 34 Circuit

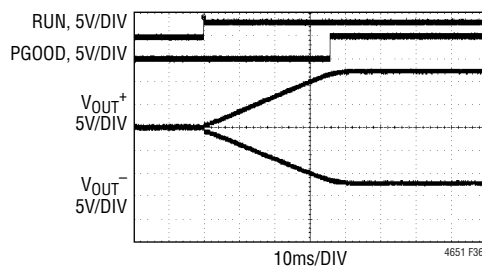
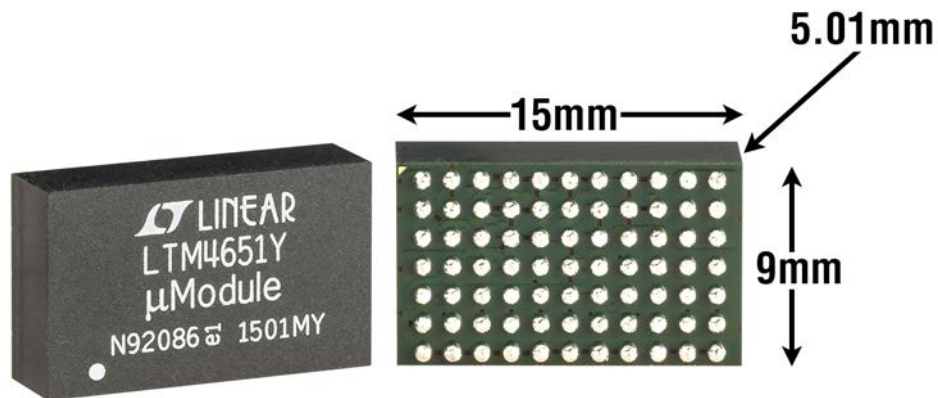


Figure 36. Concurrent  $\pm 12V$  Supply, Output Voltage Start-Up Waveforms. Figure 37 Circuit



## PACKAGE PHOTOGRAPH



## PACKAGE DESCRIPTION

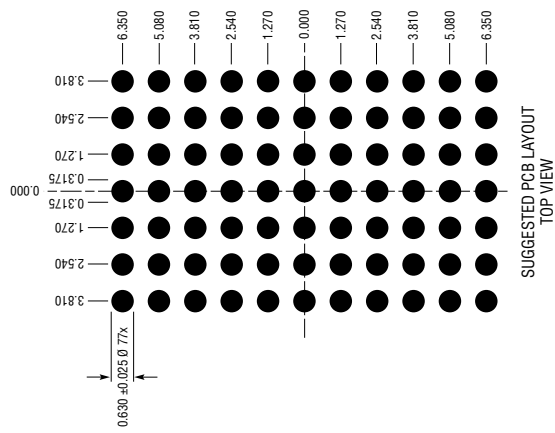
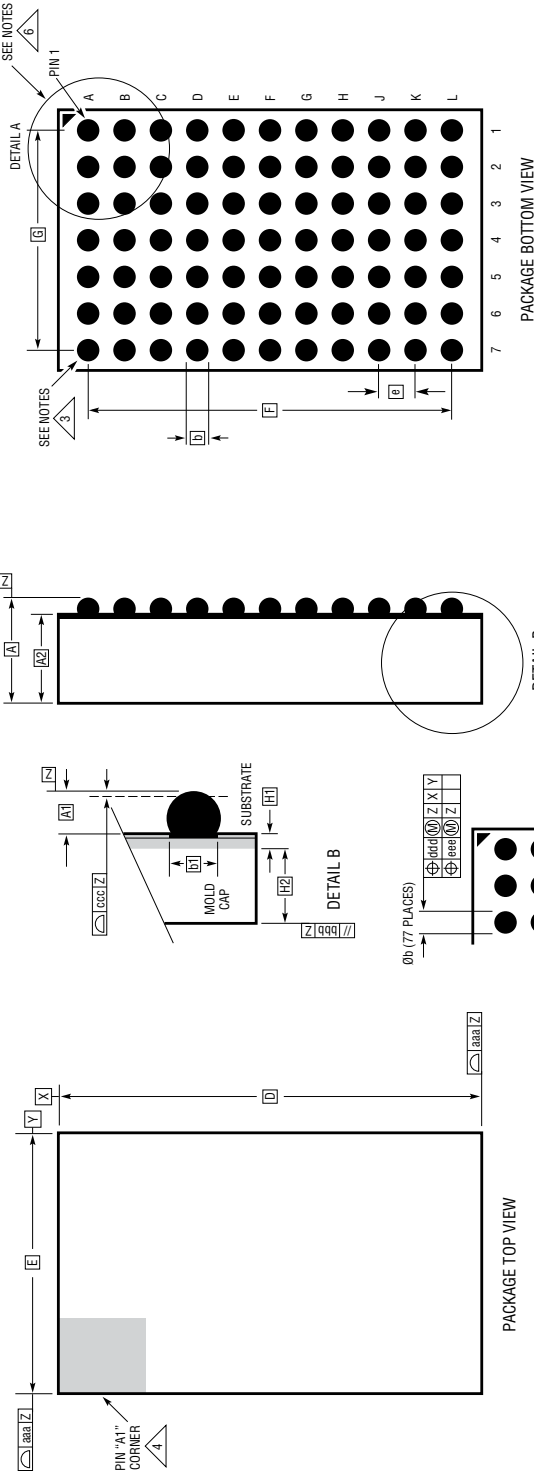
Table 9. LTM4651 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	$V_{IN}$	B1	CLKIN	C1	NC	D1	PGOOD	E1	COMPb	F1	ISETb
A2	$V_{IN}$	B2	NC	C2	$V_{OUT}^-$	D2	PGDFB	E2	COMPa	F2	ISETa
A3	$V_{IN}$	B3	$V_{IN}$	C3	$SV_{IN}$	D3	VINREG	E3	$f_{SET}$	F3	EXTV <sub>CC</sub>
A4	$V_D$	B4	$V_D$	C4	$V_D$	D4	GND	E4	$SV_{OUT}^-$	F4	RUN
A5	$V_{OUT}^-$	B5	$V_{OUT}^-$	C5	$V_{OUT}^-$	D5	$V_{OUT}^-$	E5	$V_{OUT}^-$	F5	$V_{OUT}^-$
A6	NC	B6	NC	C6	NC	D6	NC	E6	NC	F6	NC
A7	NC	B7	NC	C7	NC	D7	NC	E7	NC	F7	NC

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND <sub>SNS</sub>	H1	GND <sub>SNS</sub>	J1	TEMP <sup>+</sup>	K1	PGND	L1	PGND
G2	$SV_{OUT}^-$	H2	$SV_{OUT}^-$	J2	TEMP <sup>-</sup>	K2	PGND	L2	PGND
G3	INTV <sub>CC</sub>	H3	$V_{OUT}^-$	J3	$V_{OUT}^-$	K3	PGND	L3	PGND
G4	$V_{OUT}^-$	H4	SW	J4	$V_{OUT}^-$	K4	$V_{OUT}^-$	L4	$V_{OUT}^-$
G5	$V_{OUT}^-$	H5	$V_{OUT}^-$	J5	$V_{OUT}^-$	K5	$V_{OUT}^-$	L5	$V_{OUT}^-$
G6	NC	H6	NC	J6	TEMP <sup>+</sup>	K6	NC	L6	NC
G7	NC	H7	NC	J7	TEMP <sup>-</sup>	K7	NC	L7	NC

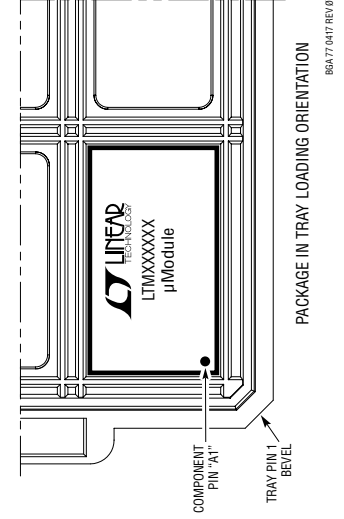
# PACKAGE DESCRIPTION

**BGA Package**  
**77-Lead (15.00mm × 9.00mm × 5.01mm)**  
 (Reference LTC DWG# 05-08-1826 Rev 0)



SYMBOL	DIMENSIONS			NOTES
	MIN	NOM	MAX	
A	4.81	5.01	5.21	BALL HT
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D	15.00			
E	9.00			
e	1.27			
F	12.70			
G	7.62			
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
				TOTAL NUMBER OF BALLS: 77

- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

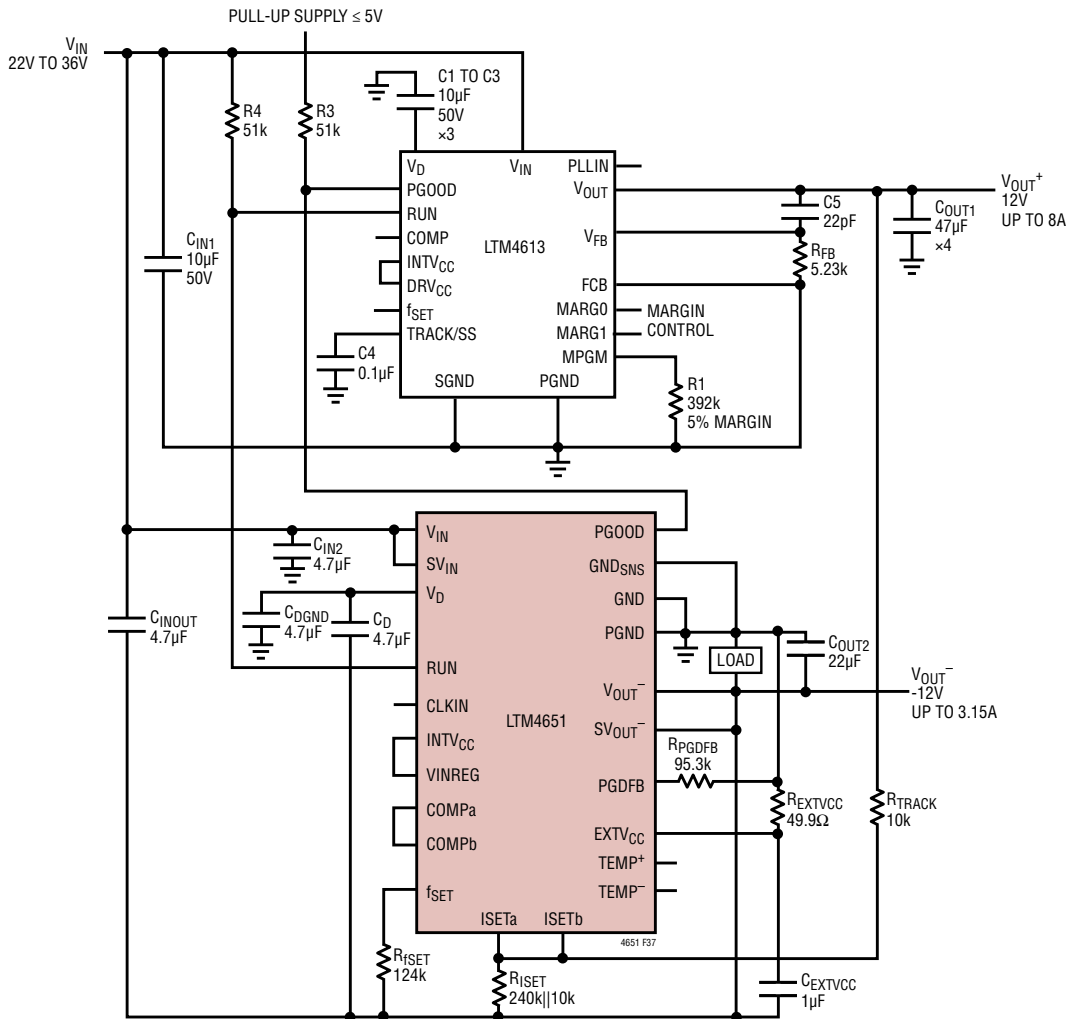


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**REVISION HISTORY**

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/16	Fixed typo on RUN Leakage Current	4

## TYPICAL APPLICATION

Figure 37. Concurrent  $\pm 12\text{V}$  Supply. See Figure 36 for Output Voltage Start-Up Waveforms

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8045	SEPIC or Inverting $\mu\text{Module}$ DC/DC Converter	$2.8\text{V} \leq V_{\text{IN}} \leq 18\text{V}$ , $\pm 2.5\text{V} \leq V_{\text{OUT}} \leq \pm 15\text{V}$ . $I_{\text{OUT}}(\text{DC}) \leq 700\text{mA}$ . $6.25\text{mm} \times 11.25\text{mm} \times 4.92\text{mm}$ BGA
LTM8049	Dual, SEPIC and/or Inverting $\mu\text{Module}$ DC/DC Converter	$2.6\text{V} \leq V_{\text{IN}} \leq 20\text{V}$ , $\pm 2.5\text{V} \leq V_{\text{OUT}} \leq \pm 24\text{V}$ . $I_{\text{OUT}}(\text{DC}) \leq 1\text{A}/\text{Channel}$ . $9\text{mm} \times 15\text{mm} \times 2.42\text{mm}$ BGA
LTM8073	60V, 3A Step-Down $\mu\text{Module}$ Regulator	$3.4\text{V} \leq V_{\text{IN}} \leq 60\text{V}$ , $0.8\text{V} \leq V_{\text{OUT}} \leq 15\text{V}$ . $6.25\text{mm} \times 9\text{mm} \times 3.32\text{mm}$ BGA
LTM8064	58V, $\pm 6\text{A}$ CVCC Step-Down $\mu\text{Module}$ Regulator	$6\text{V} \leq V_{\text{IN}} \leq 58\text{V}$ , $1.2\text{V} \leq V_{\text{OUT}} \leq 36\text{V}$ . $11.9\text{mm} \times 16\text{mm} \times 4.92\text{mm}$ BGA
LTM4613	EN55022B Compliant, 36V, 8A $\mu\text{Module}$ Regulator	$5\text{V} \leq V_{\text{IN}} \leq 36\text{V}$ , $3.3\text{V} \leq V_{\text{OUT}} \leq 15\text{V}$ . $15\text{mm} \times 15\text{mm} \times 4.32\text{mm}$ LGA, and $15\text{mm} \times 15\text{mm} \times 4.92\text{mm}$ BGA

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